An innovative Vision System for Industrial Applications

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Supervised by: Prof. Javier Garrido Salas

Outline

Introduction

Goals

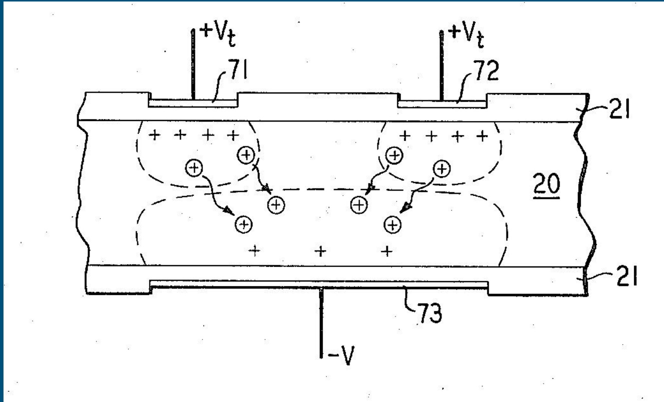
Requirement Analysis

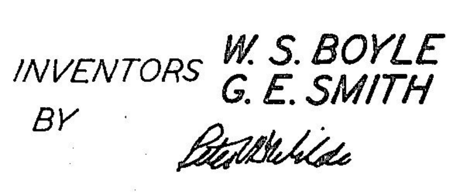
Generic Computer Vision System

Validation

Conclusion and future work

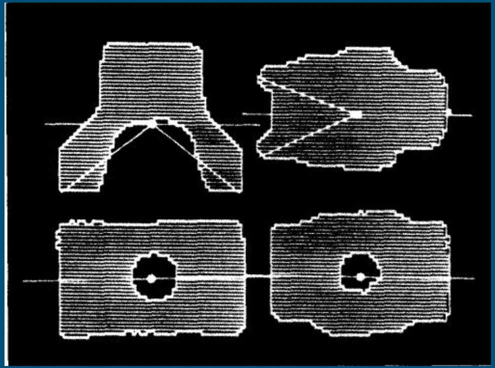
Creation of the CCD

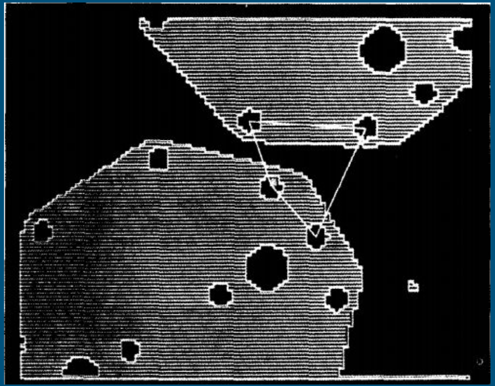


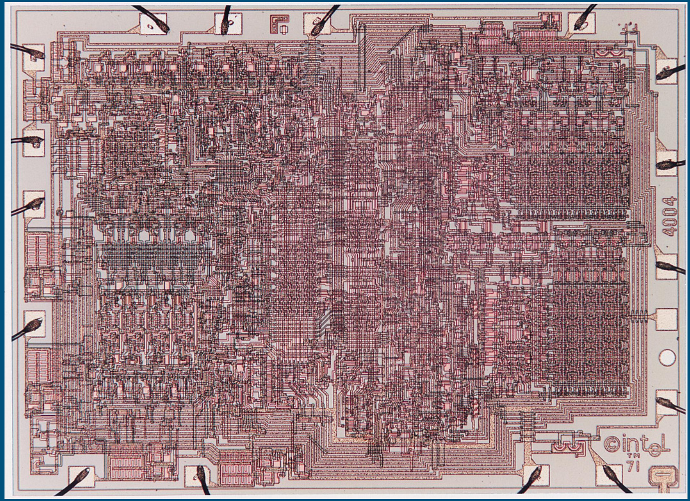


1969

SRI Vision Module







1972

Custom-designed computer vision systems are being applied to specific manufacturing tasks. Current development may lead to general-purpose systems for a broad range of industrial applications.

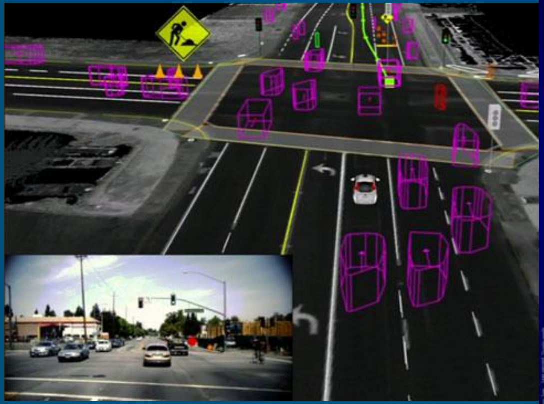
Gerald J. Agin, 1980

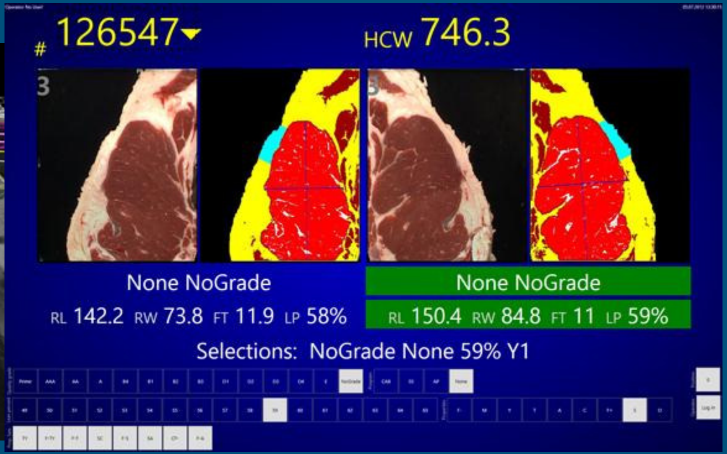
Stanford Research Institute

Agin, Gerald J. "Computer vision systems for industrial inspection and assembly." *Computer* 5 (1980): 11-20.

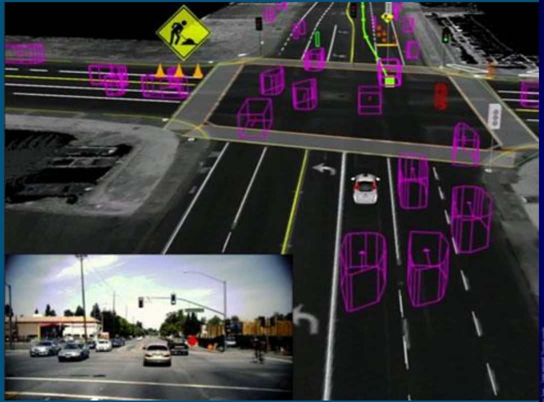
Computer Vision Today

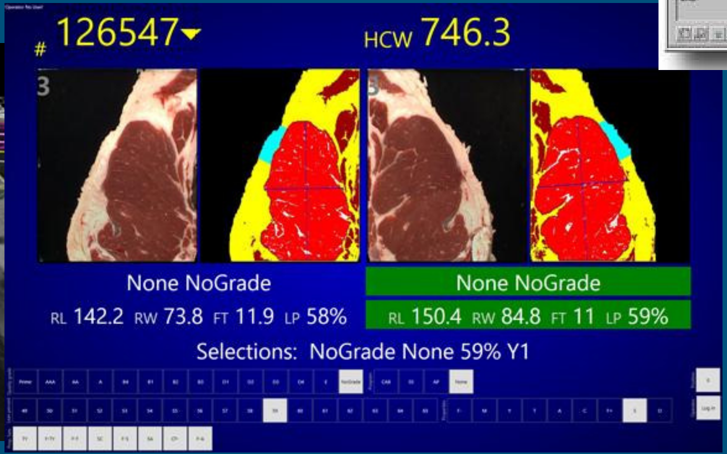
Computer Vision Today



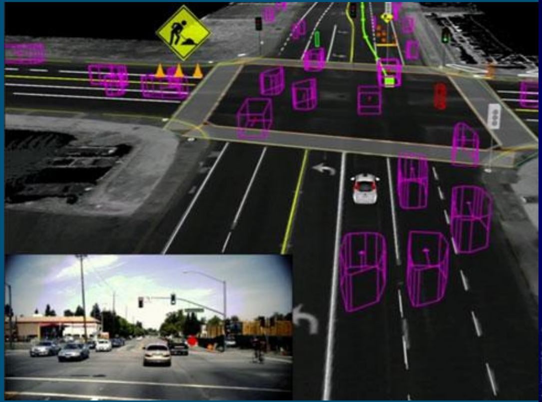


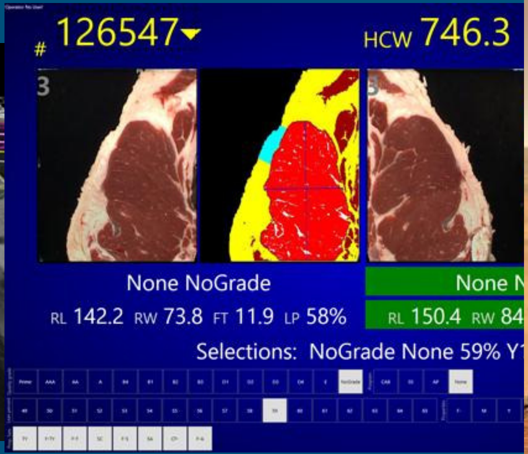
Computer Vision Today



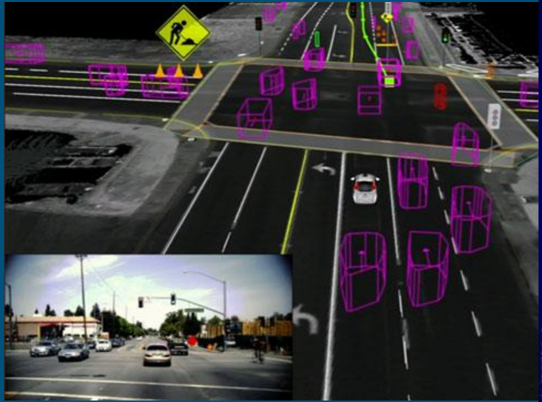


Computer Vision Today

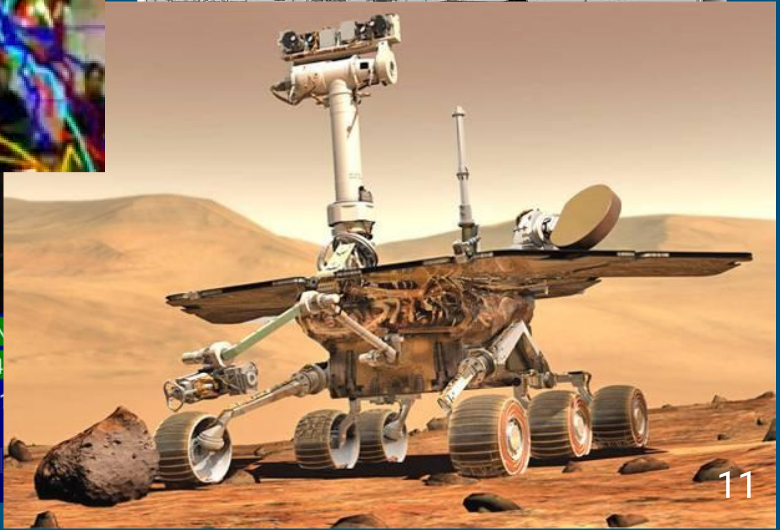




Computer Vision Today



Computer Vision Today



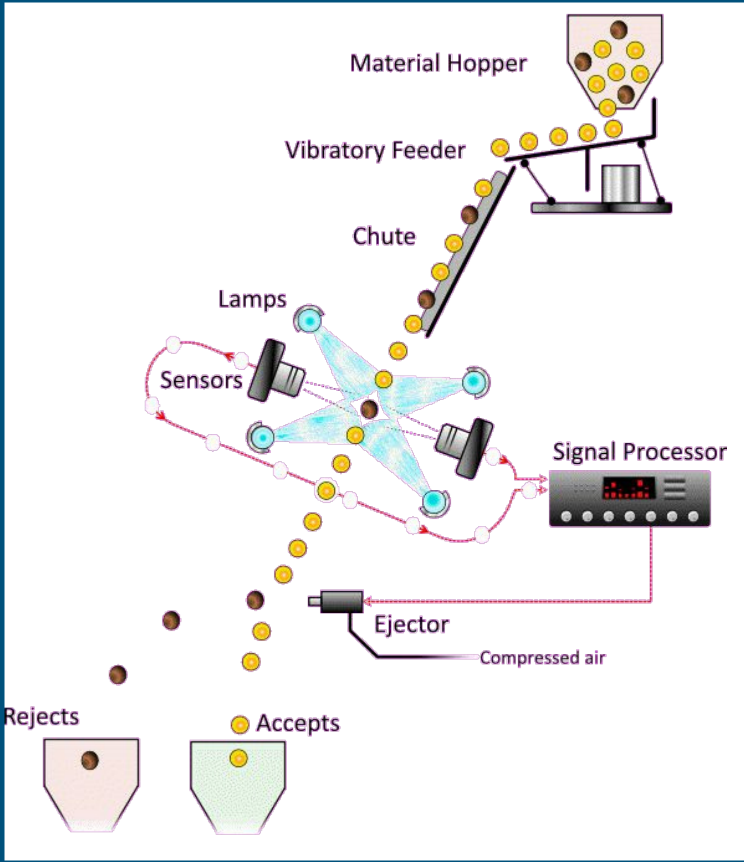
Industrial Computer Vision

Great computing demands

Low latency

High profit margin

New opportunities every day



Application Development

Multidisciplinary

Uncertaint

Closed market

Incomparable results

Single use components

Goals

General Purpose Computer Vision System

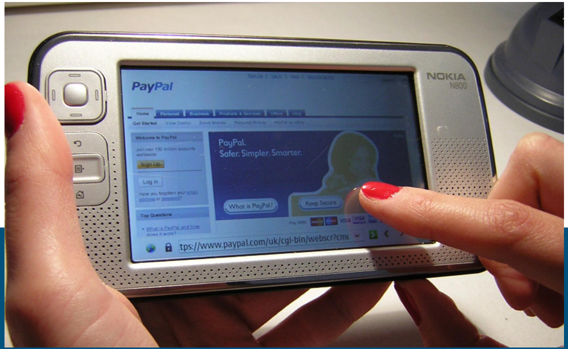
Reusable parts

Comparable results

Wide Spectrum of applications

Based on Open Source

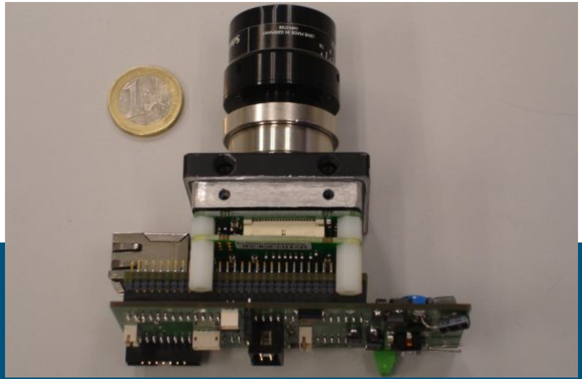
Requirement Analysis



System on Chip

Biometric System on Token

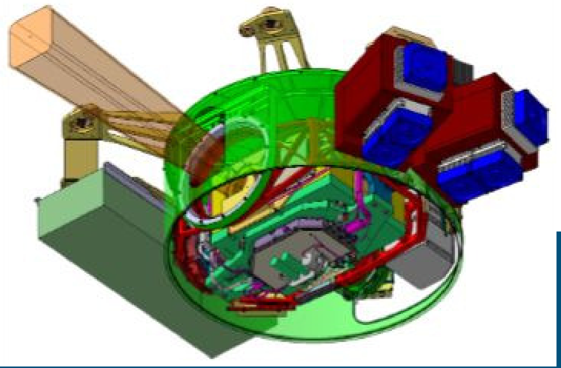
Texas OMAP4 SOC



FPGA

Fingerprint Acquisition System

Virtex 4 FPGA



CPU + GPU

Bidimensional Interferometer

Nvidia Tesla GPU

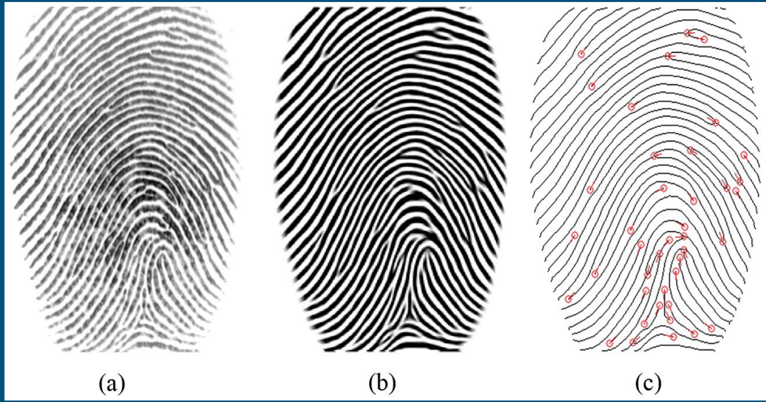
System on Chip Computer Vision System

Application: Fingerprint matching

Hardware: Nokia N800 based on Texas Instruments OMAP 3 SOC

Software: NBIS fingerprint processing software

Goal: 2 seconds per transaction



System on Chip Computer Vision System

Pros

Auditable Open Source stack

Integrated DSP

Mature API

COTS Hardware

Cons

Small selection of sensors

Limited computer resources

Non updatable hardware

No direct access to the sensor

FPGA Computer Vision System

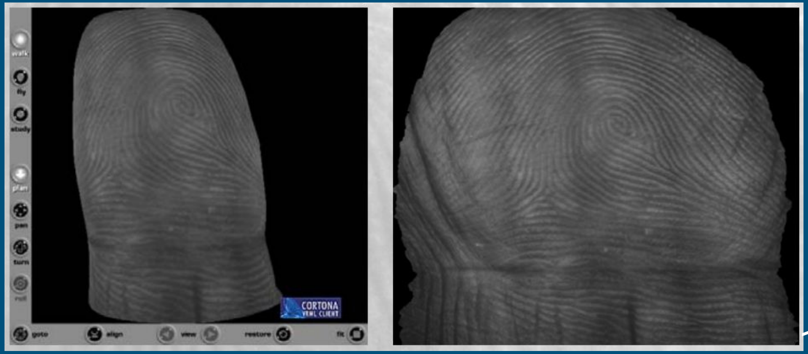
Application: Acquisition of fingerprints in 3D

Sensor: Vector BCI 6 Mpix Mono

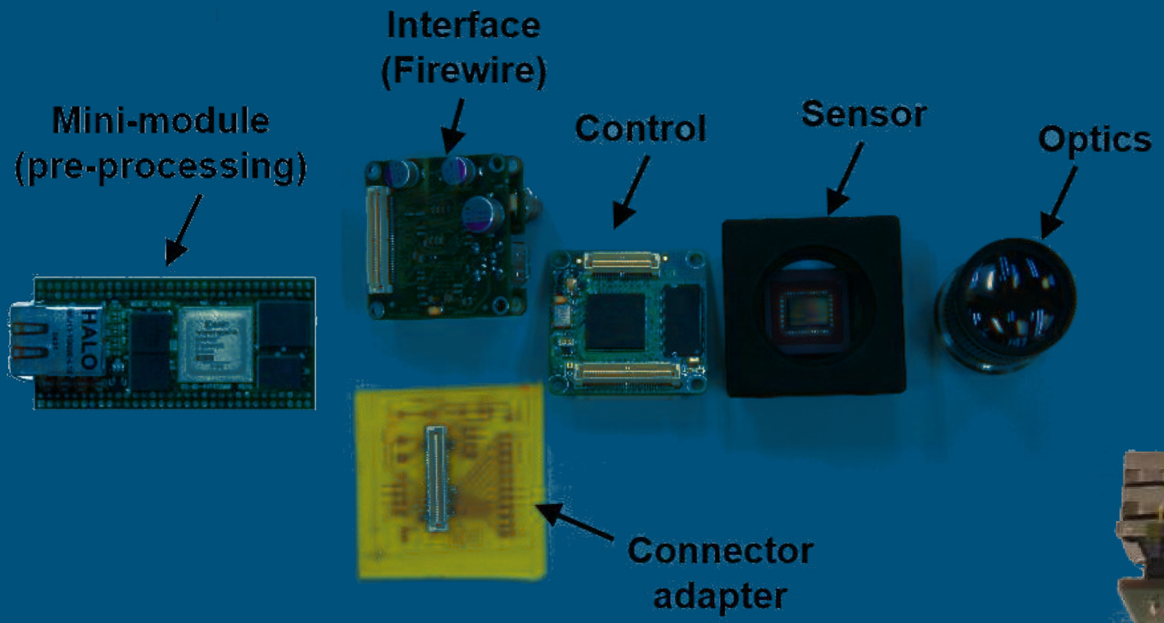
Hardware: Custom System based on Virtex 4 FX FPGA

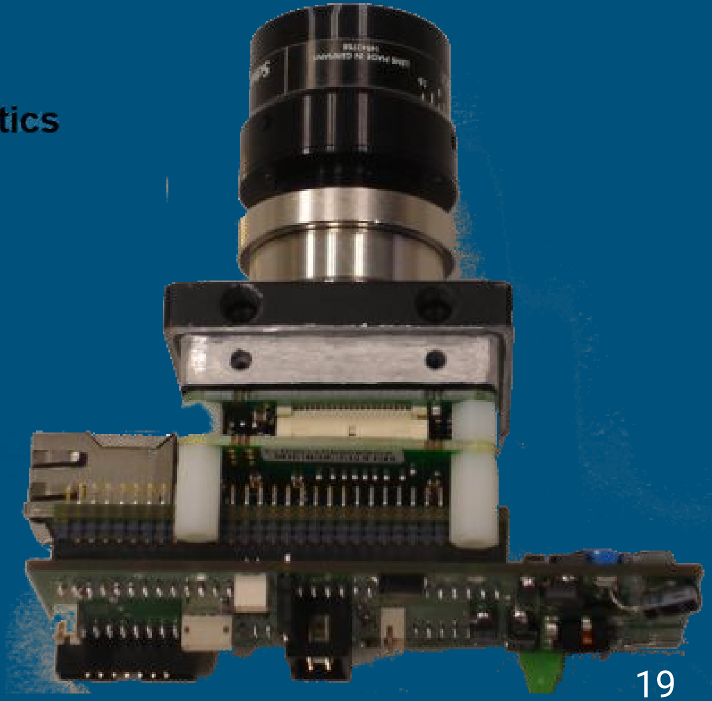
Software: Custom Linux Distribution

Goals: Low latency auditable



FPGA Computer Vision System





FPGA Computer Vision System

NIJ | National Institute of Justice

TBS

DEPARTMENT OF JUSTICE
QUI PRO DOMINA JUSTITIA SEQUITUR

Used on real life

FPGA Computer Vision System

Pros

Image Preprocessing Capabilities

Low level access to the sensor

Open Source Stack

Cons

Highly coupled to the selected sensor

Low Performance CPU

Custom sensor API

No Image Processing Software Stack

Slow Development Cycle

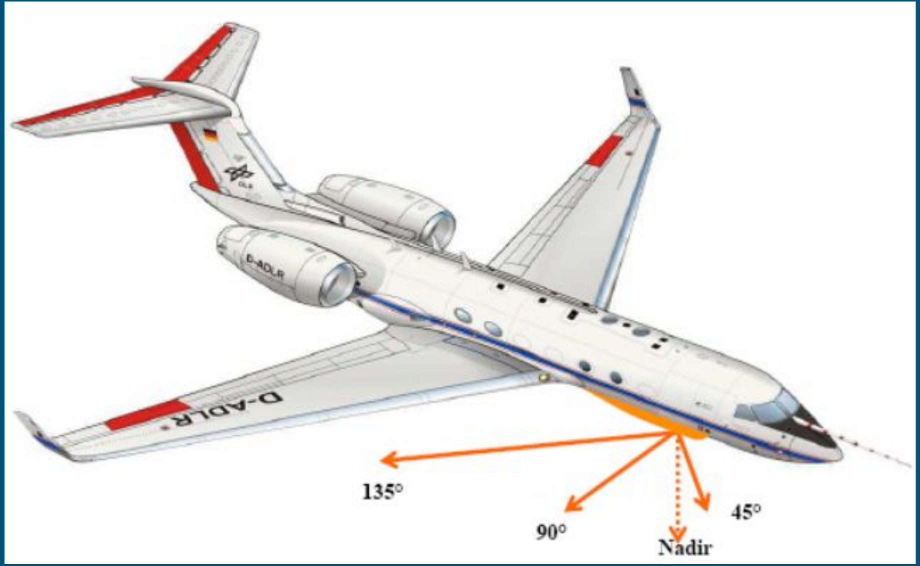
GPU + CPU Computer Vision System

Application: Atmospheric research

Hardware: x86 + NVIDIA GPU

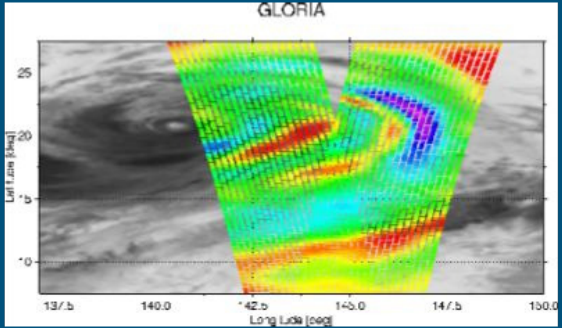
Software: C+CUDA

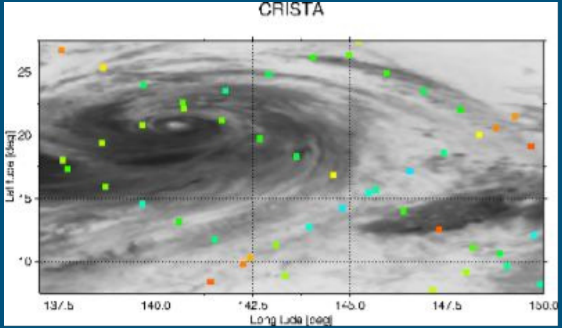
Goal: real time processing

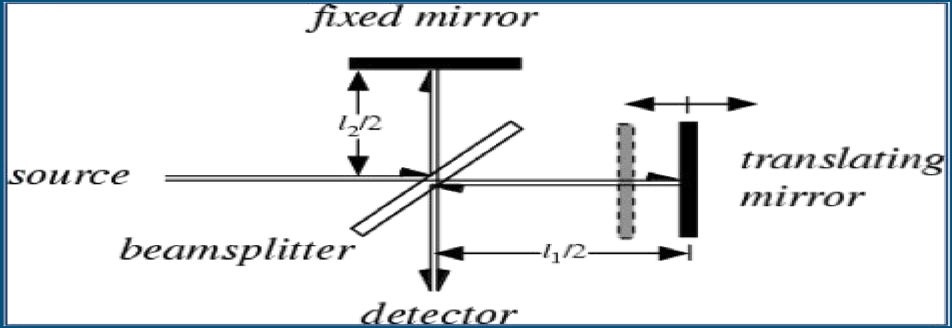


JÜLICH
FORSCHUNGSZENTRUM

GPU + CPU Computer Vision System







GPU + CPU Computer Vision System

Pros

Great computing power

- High level of parallelization
- 200x faster than reference implementation

Simple programming (C based)

Cons

Lack of Computer Vision Stack

No image preprocessing

Highly coupled to the selected sensor

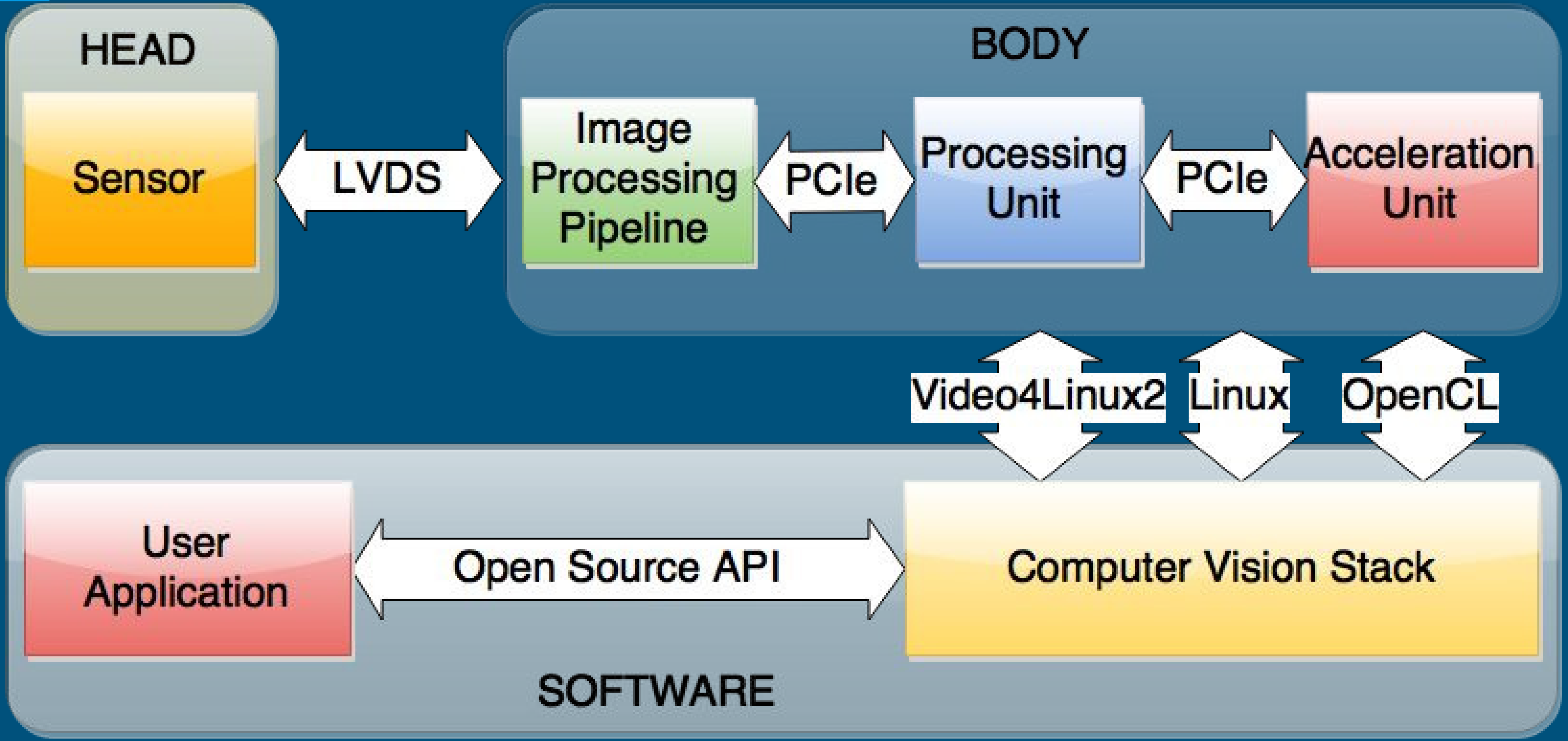
Nvidia specific programming language

★ Used on real life

Generic Computer Vision System

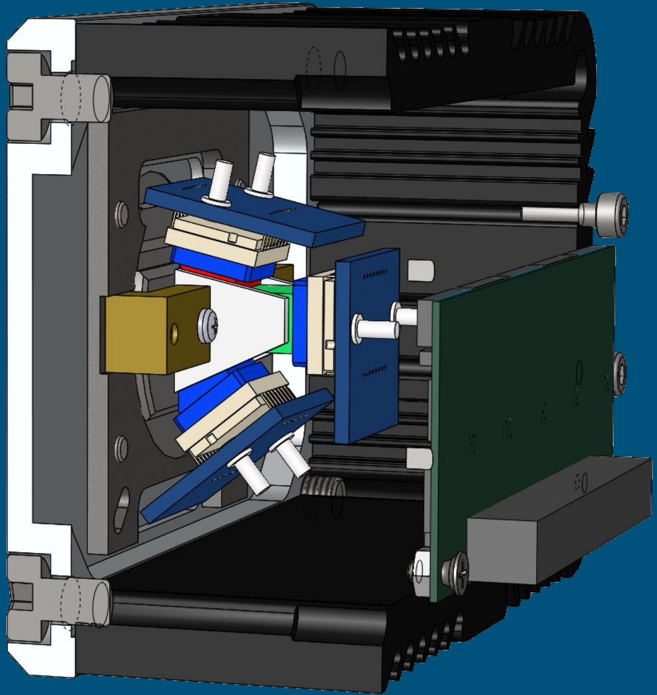
Modular Structure

Original Contribution



QT5022

QT5022: head



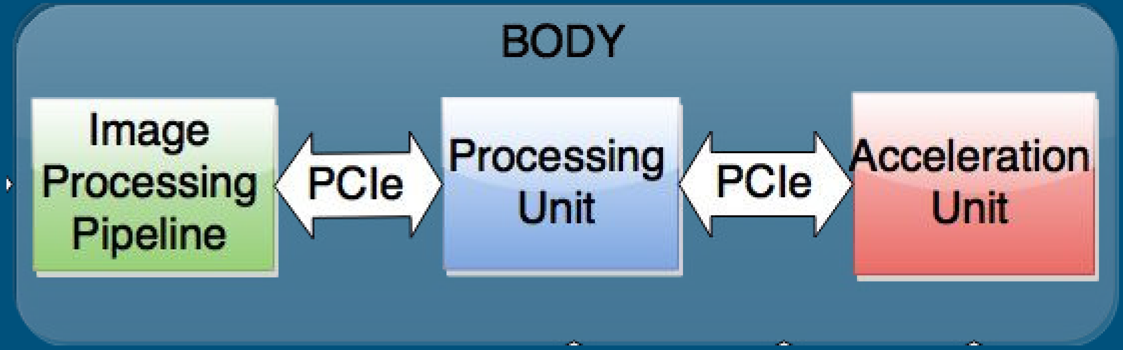
CCD: 1, 3 and 5 sensors

CMOS: 2, 4, 8 and 12 Mpix

Roic: InGaAs and microbolometer

Dual eye: CMOS

Hardware


BODY
Image Processing Pipeline
PCIe
Processing Unit
PCIe
Acceleration Unit

QT5022: body

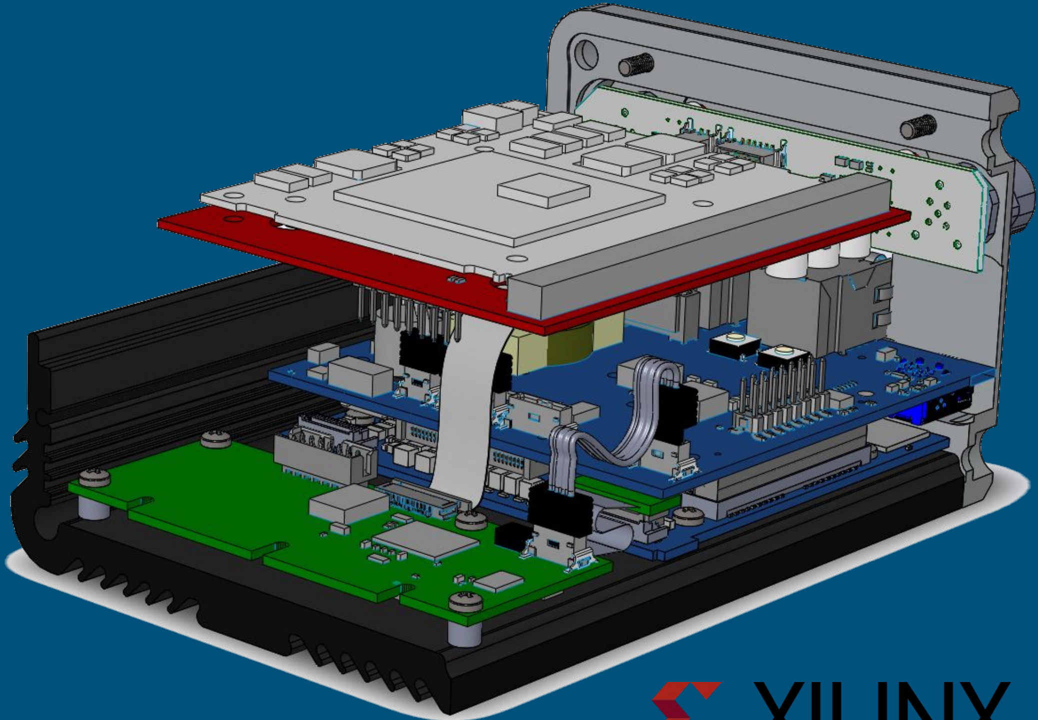


Image processing pipeline:

Spartan 6 / Kintex

Processing unit: AMD APU

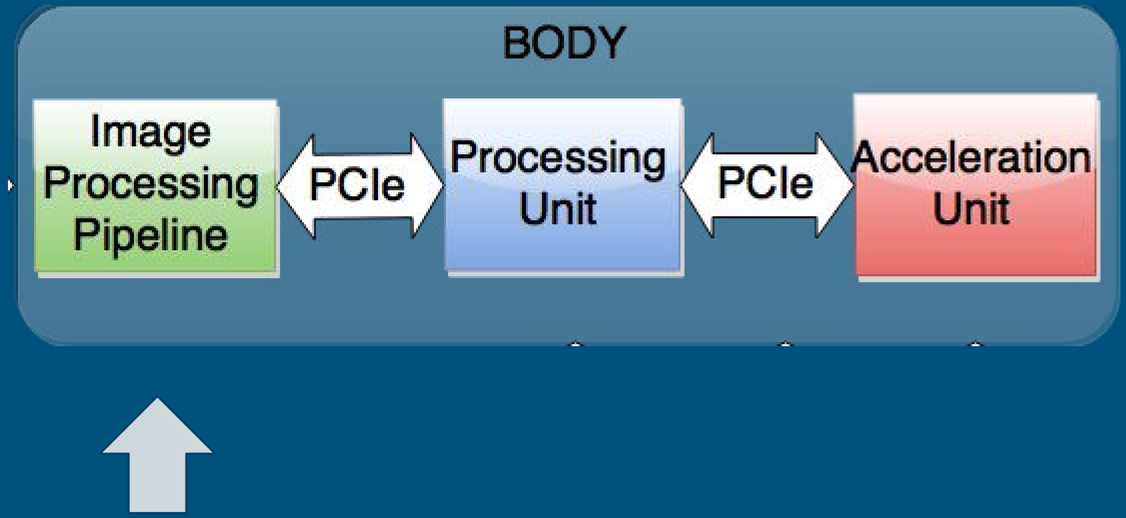
Acceleration unit: GPU

XILINX

AMD The future is fusion

AMD RADEON GRAPHICS

Hardware



BODY
Image Processing Pipeline
PCIe
Processing Unit
PCIe
Acceleration Unit

Image Processing Pipeline

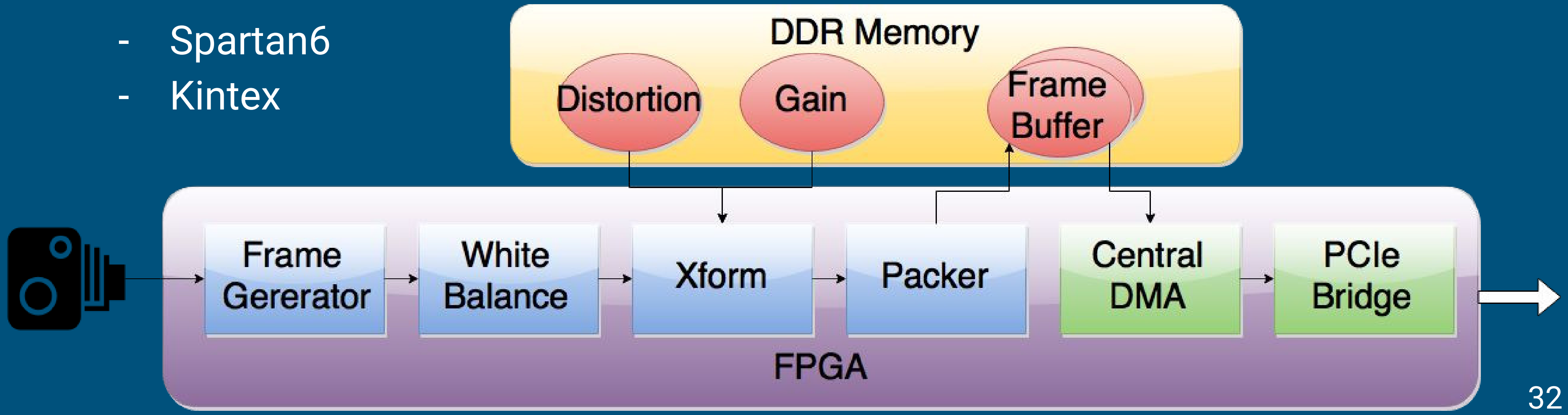
PCIe interface to the Processing Unit

2 implementations:

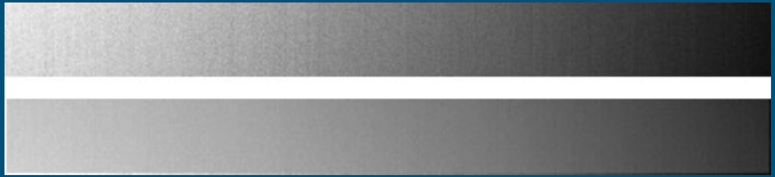
- Spartan6
- Kintex

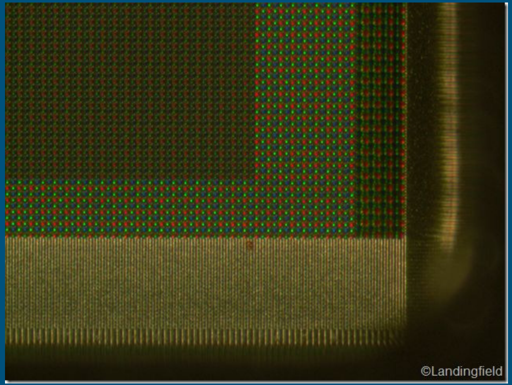
Plenty of resources available

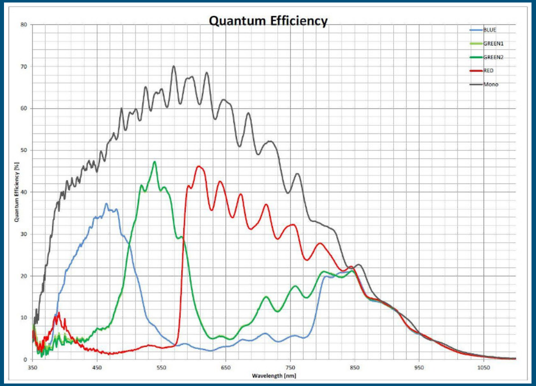
Reconfigurable



Frame Generator







Sensor Abstraction

Synchronization

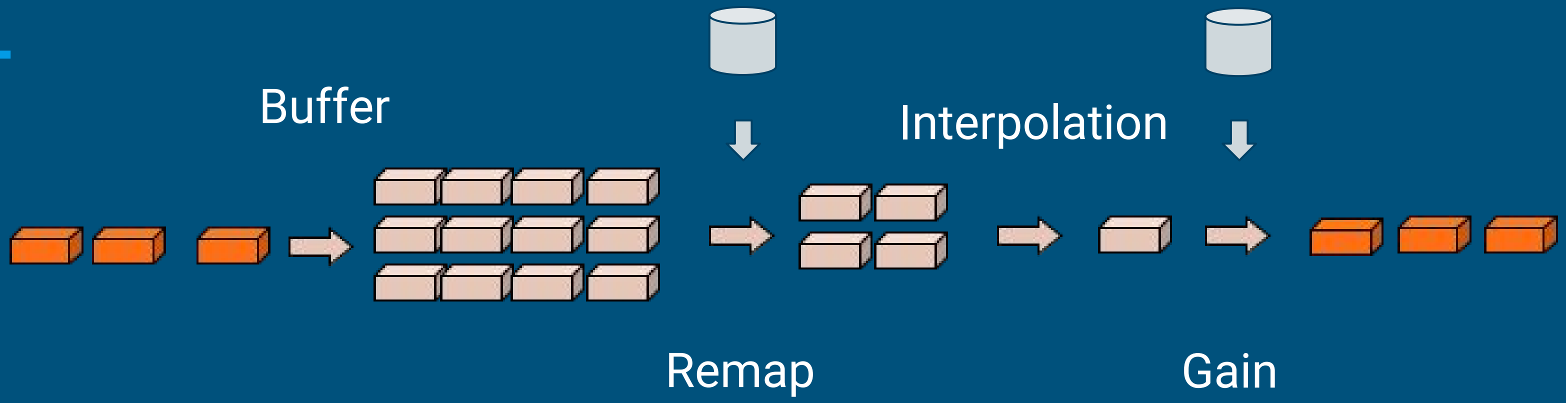
Data readout

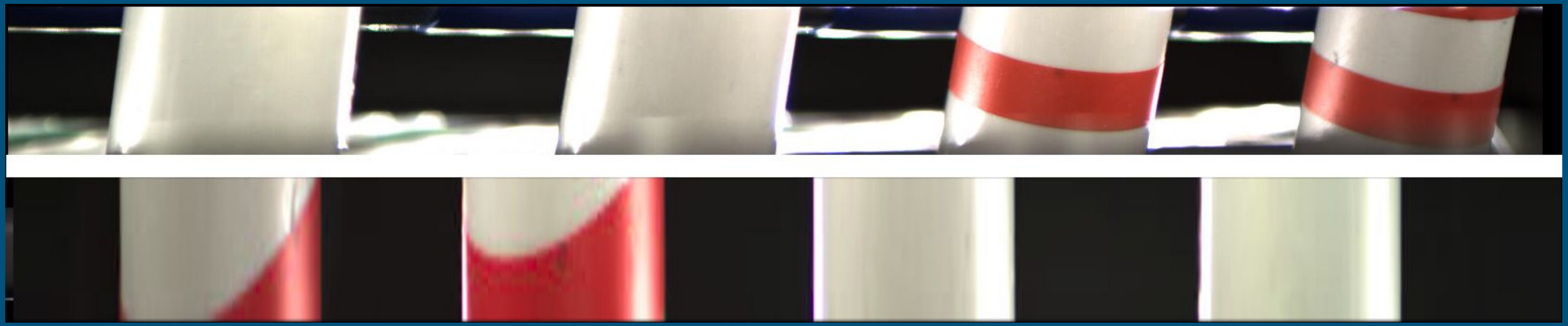
Debayer

Fixed Pattern Noise

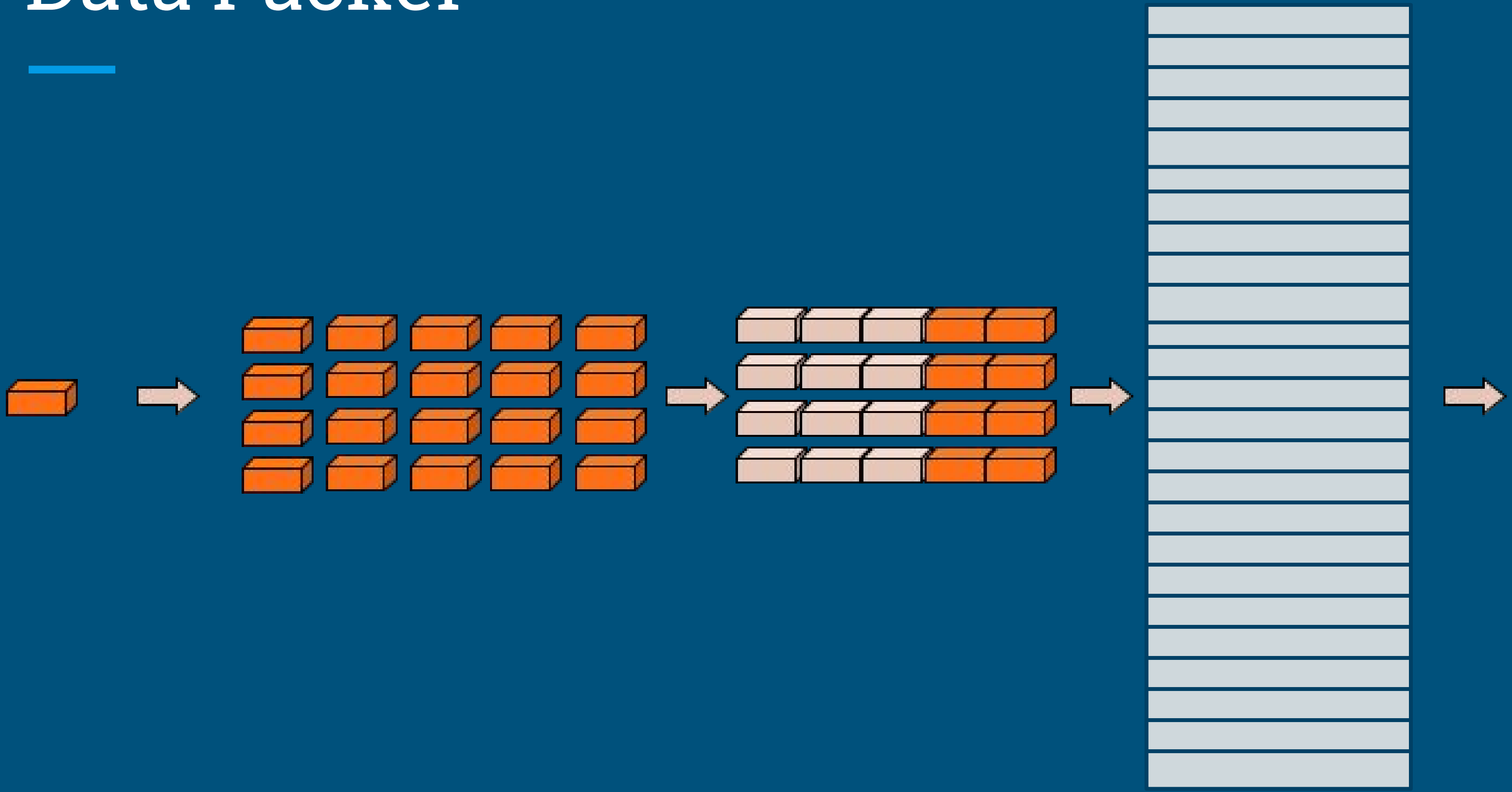
XForm

Original Contribution



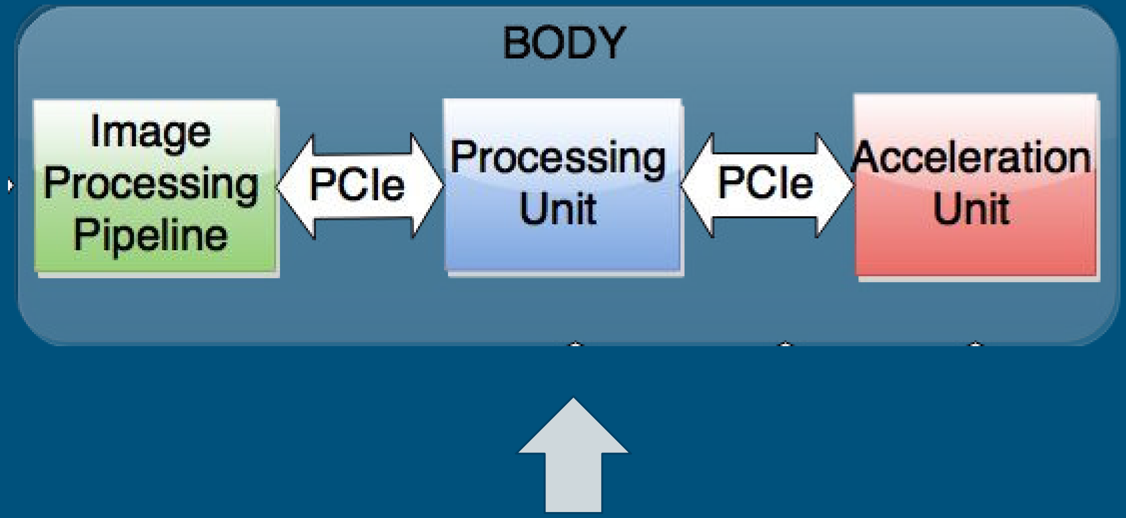


Data Packer



RGB24
RGB32
BGR24
BGR32
GREY
Y16
Y16_BE
SBGGR8
SGBRG8
SGRBG8
SRGGB8
UYVY
YUYV
RGBPP40
RGBPP80

Hardware


BODY
Image Processing Pipeline
PCIe
Processing Unit
PCIe
Acceleration Unit

Processing Unit

AMD APU G-T65N:

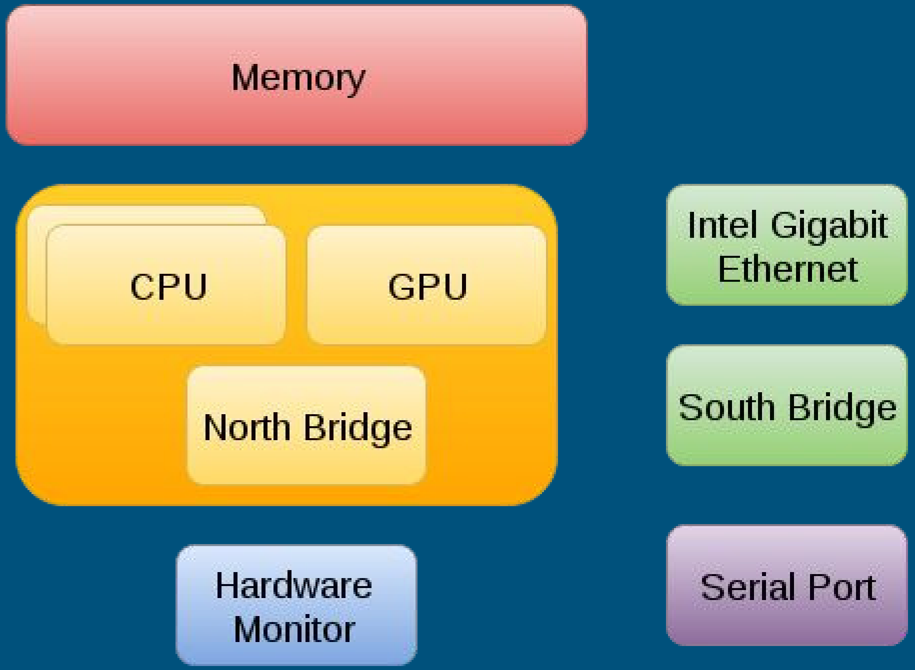
- 2 x 1.65 GHz x86 cores
- 1x Radeon 6320 GPU

Memory: 4 GiB DDR2 RAM

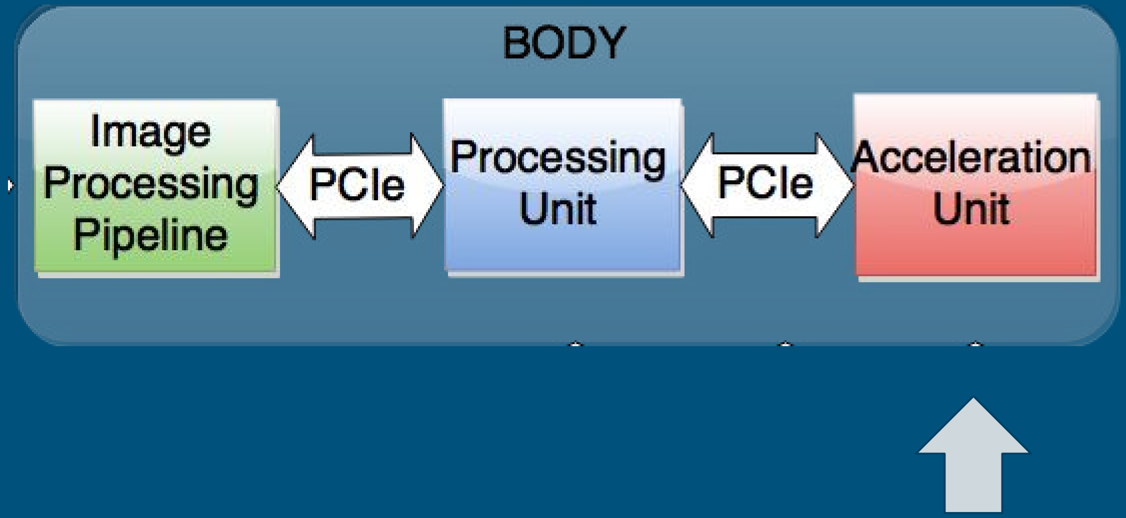
Dual Port Intel Gigabit Ethernet

Fintek Serial Port

Custom Hardware Monitor



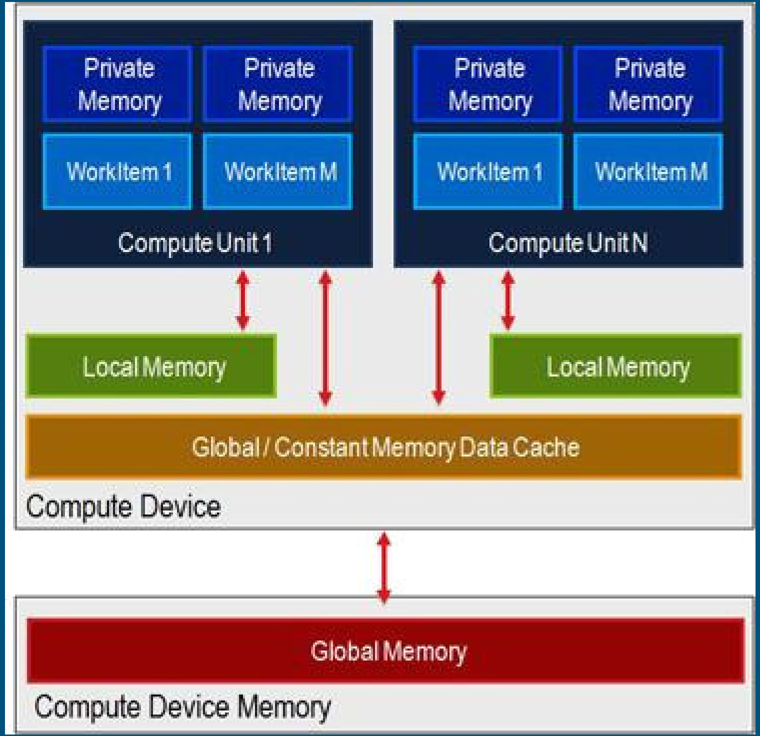
Hardware


BODY
Image Processing Pipeline
PCIe
Processing Unit
PCIe
Acceleration Unit

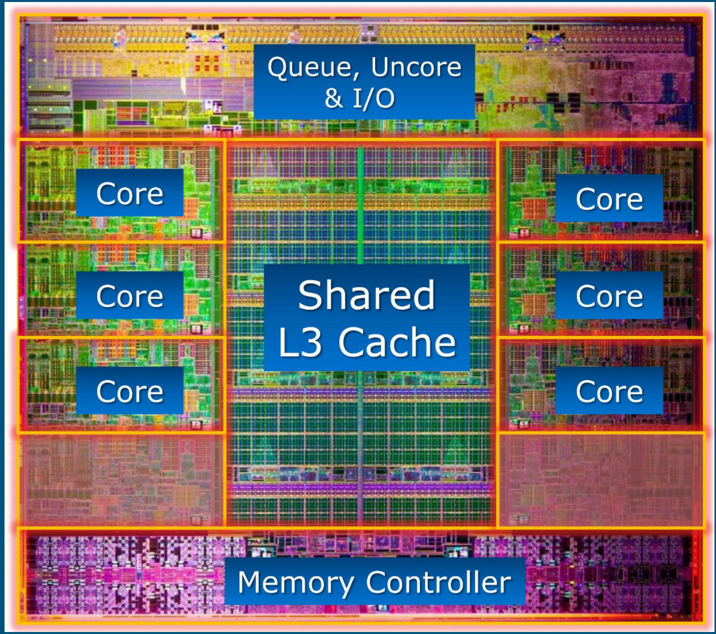
Acceleration Unit / OpenCL

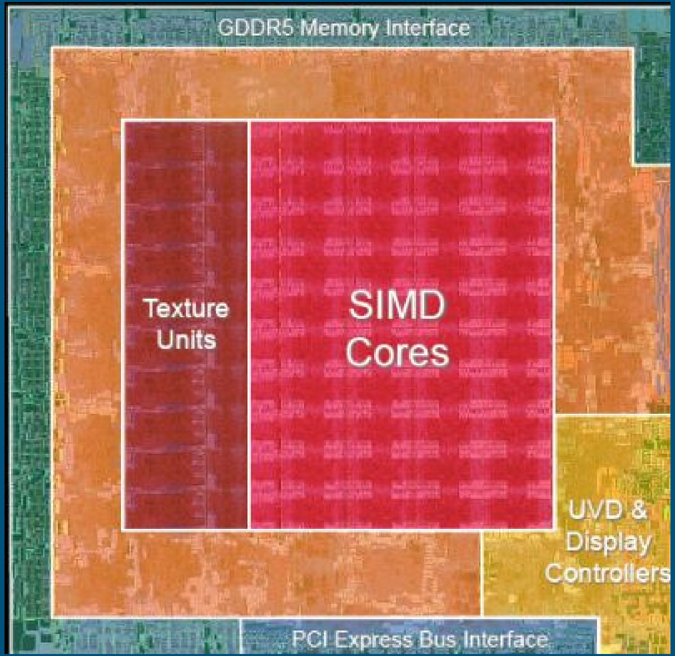
Massive number of threads

Hardware agnostic: Implemented by GPU, DSP, CPU or FPGA

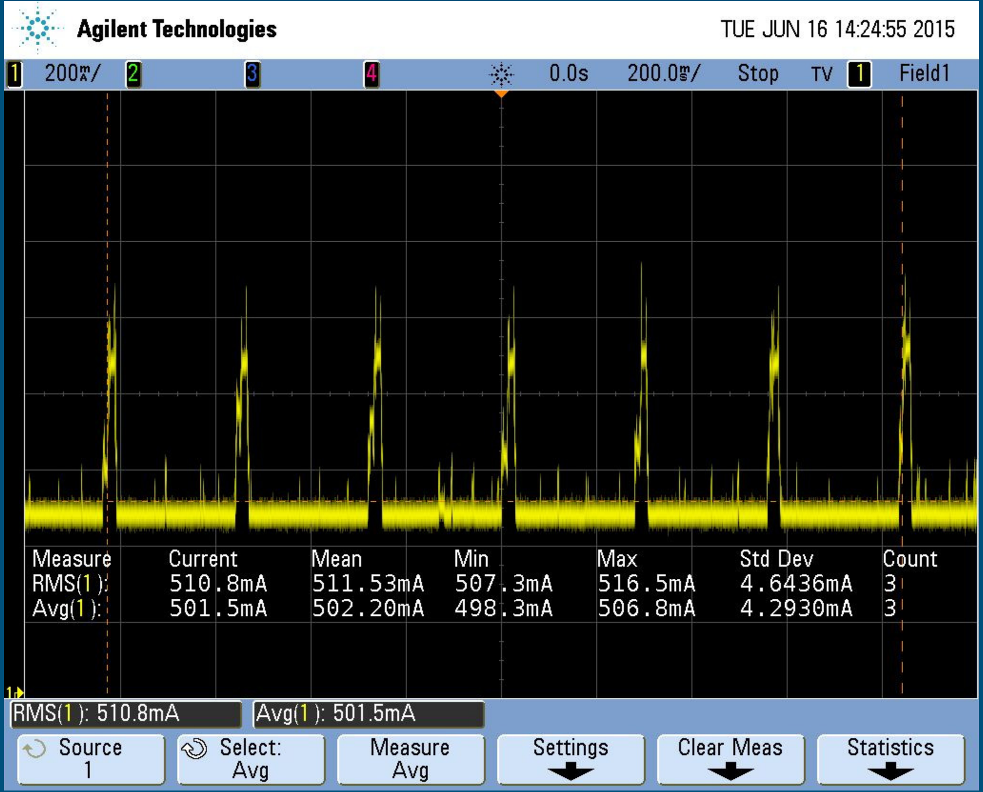


Acceleration Unit

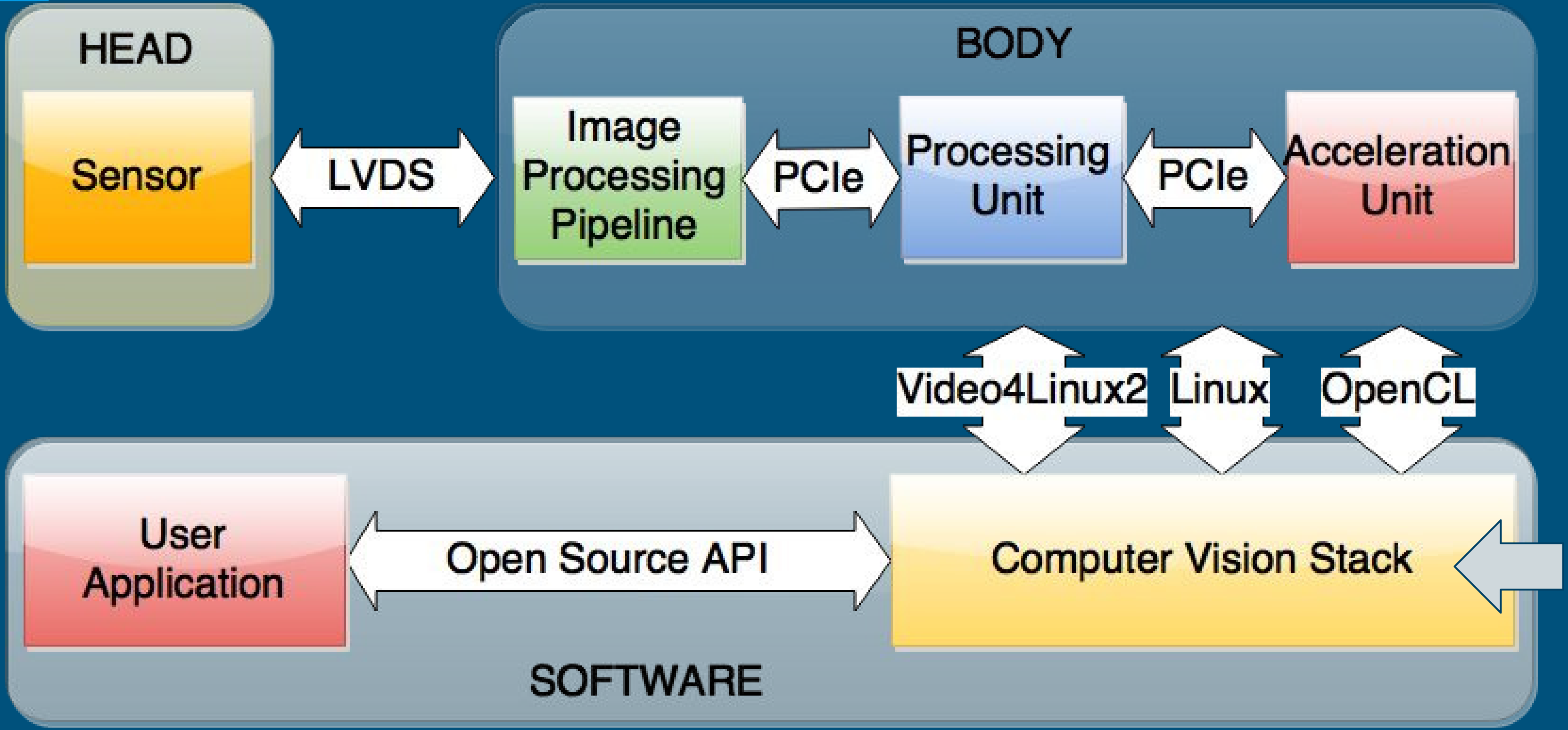




Acceleration Unit

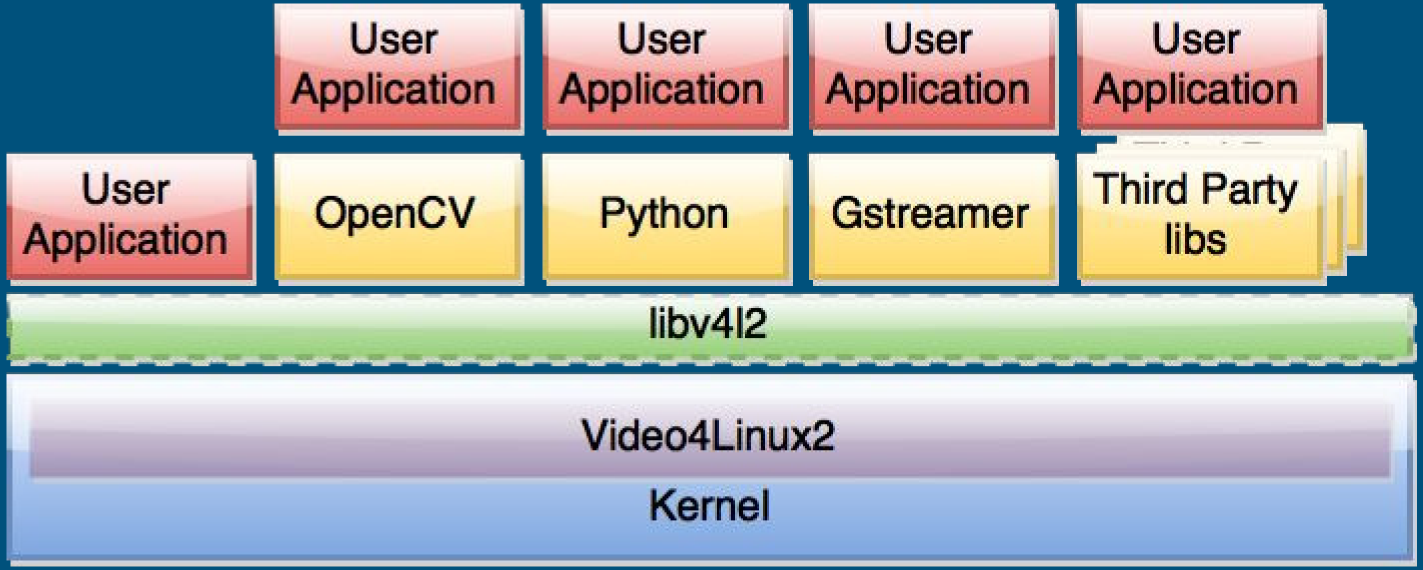


Modular Structure



Software

Original Contribution



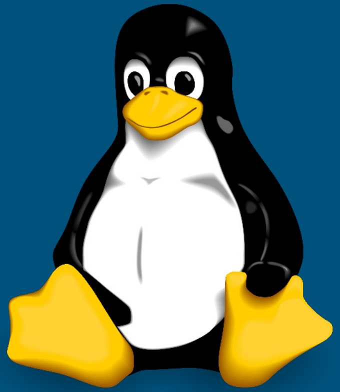
Kernel

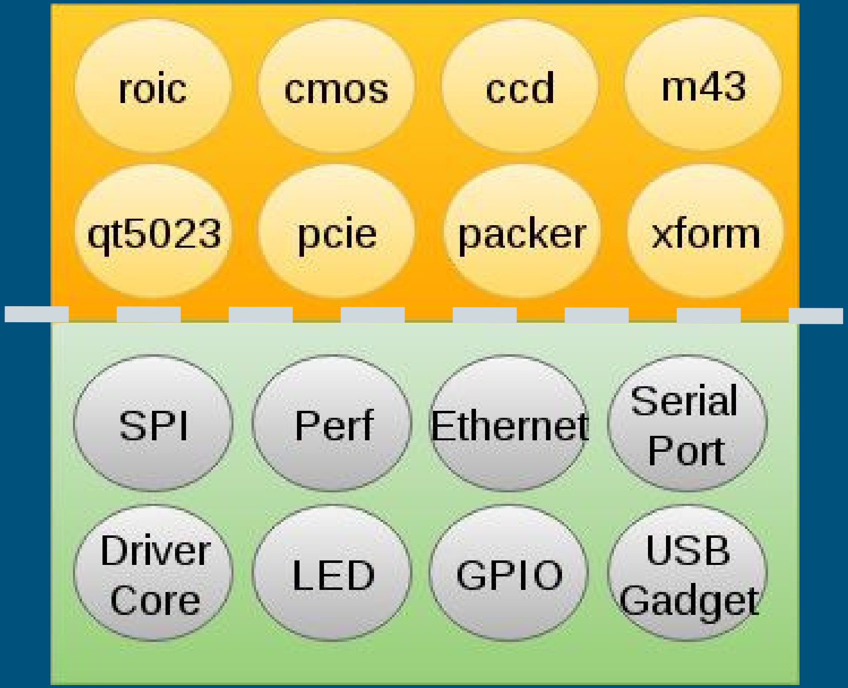
All Open Source

(except video drivers)

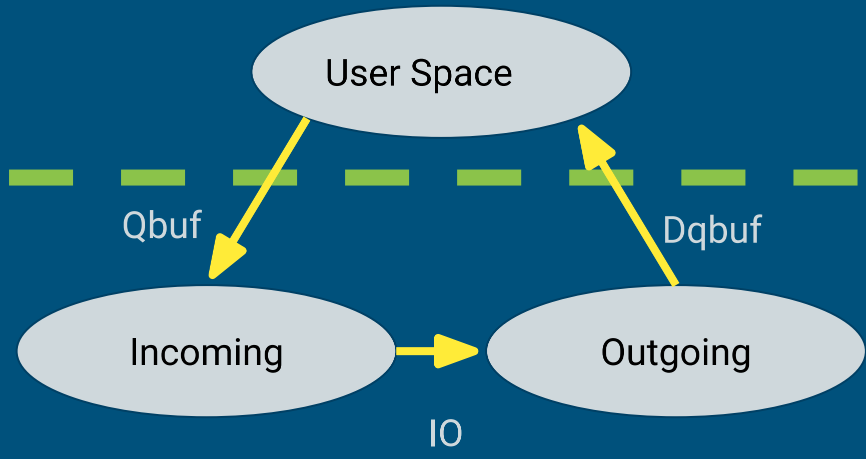
2 approaches:

- manufacturer tree
- upstream





Video4Linux



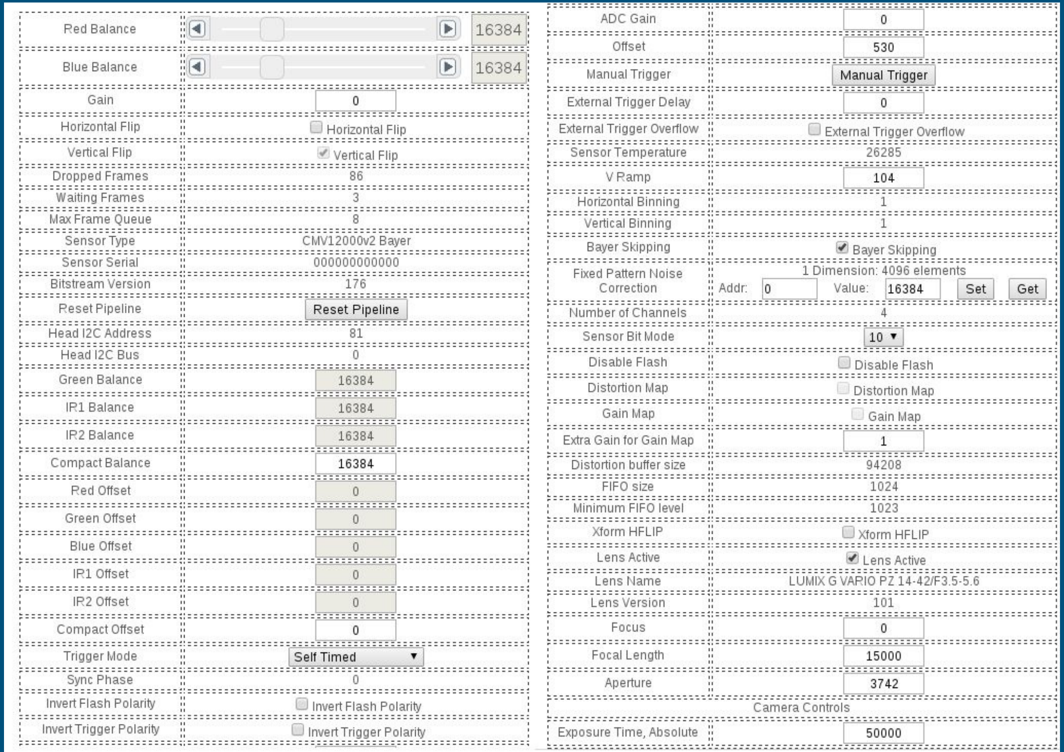
Read/Write

Memory Map

★ Userptr

Dmabuf

Video4Linux



Multitype

Cache

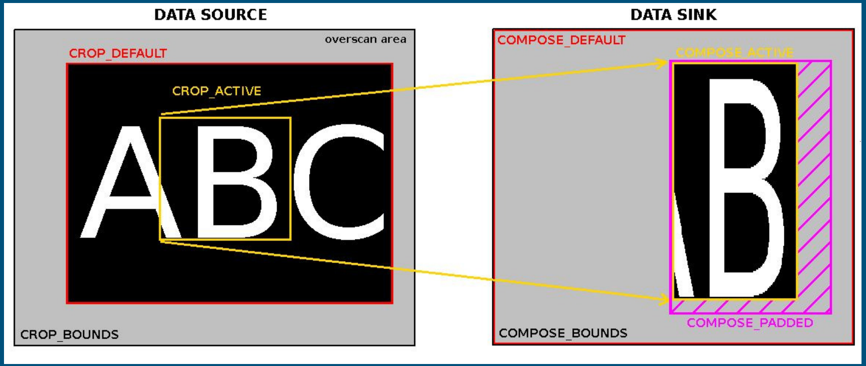
Atomic

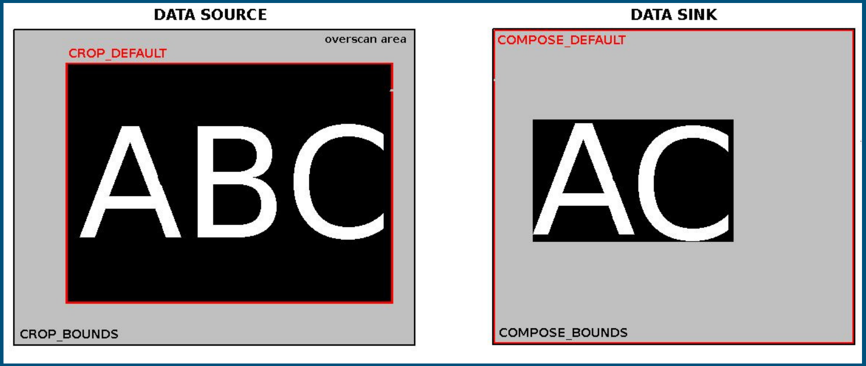
Arrays

Events

Error Flags ★

Video4Linux





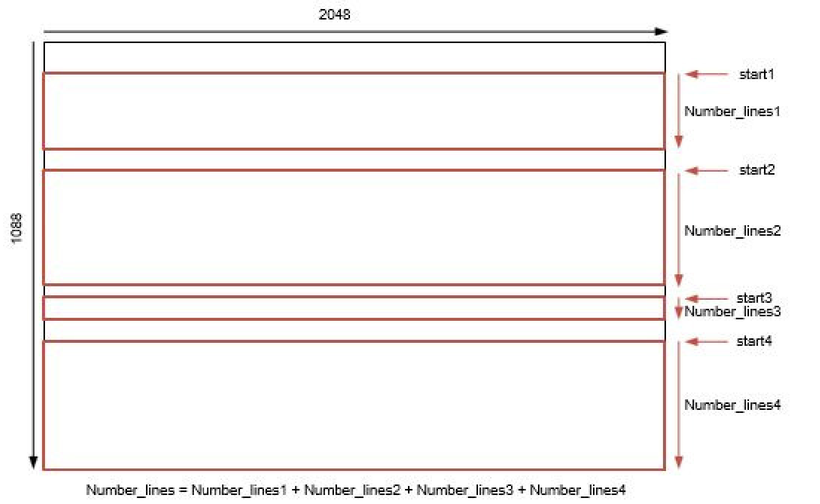
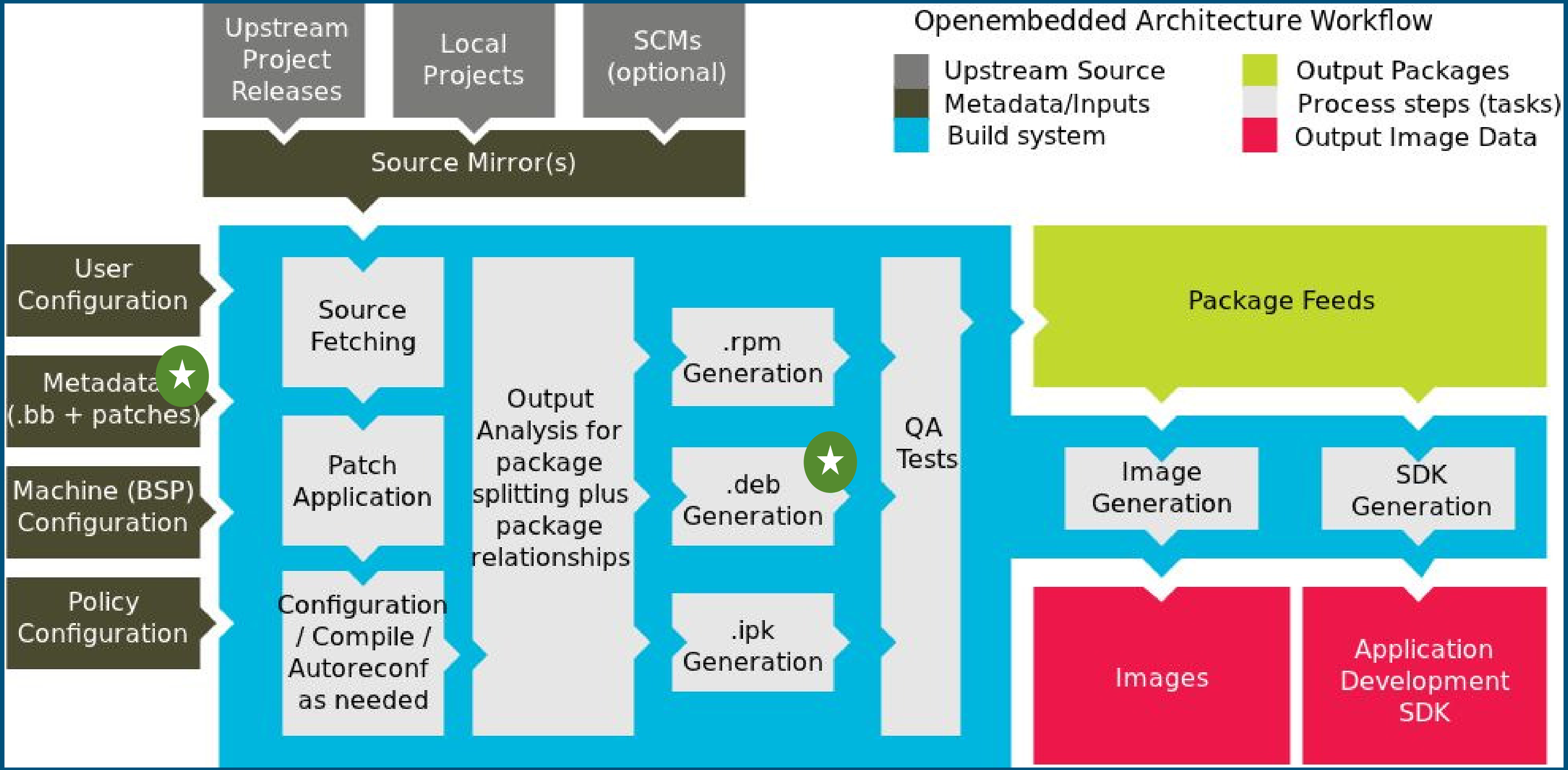


FIGURE 39: EXAMPLE OF 4 MULTIPLE FRAMES READ-OUT

Yocto Project



Computer Vision Stack

IP[y]: Notebook

OpenCL

OpenCV

gstreamer

LINUX TV

HALCON

the Power of Machine Vision

NEUROtechnology

Biometric and Artificial Intelligence Technologies

Goals Recap

Pros

Auditable Open Source stack

Integrated DSP

Mature API

Image Preprocessing Capabilities

Real time performance

Highly Parallel Architecture

Easy Programming

~~COTS Hardware~~

Cons

~~Small selection of sensors~~

~~Limited computer resources~~

~~Non updatable hardware~~

~~No direct access to the sensor~~

~~No image preprocessing~~

~~Custom sensor API~~

~~No Image Processing Software Stack~~

~~Slow Development Cycle~~

Business Model

Applications

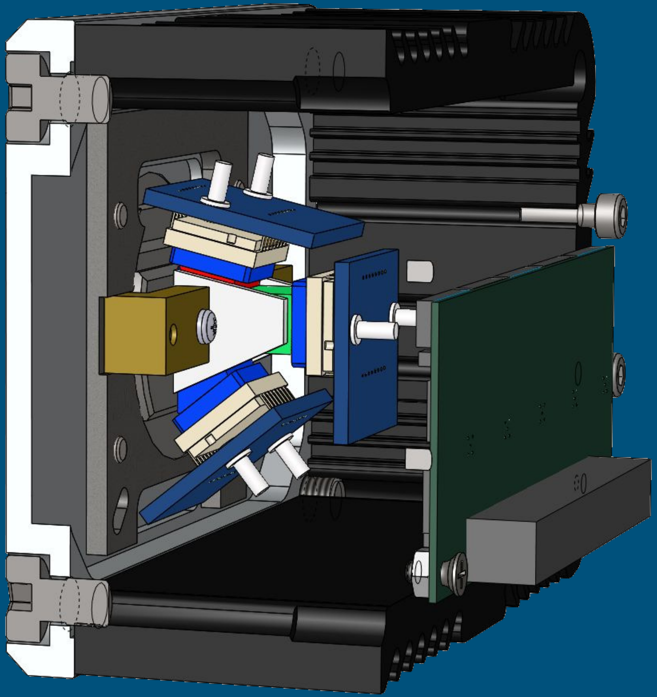
Potato Grader

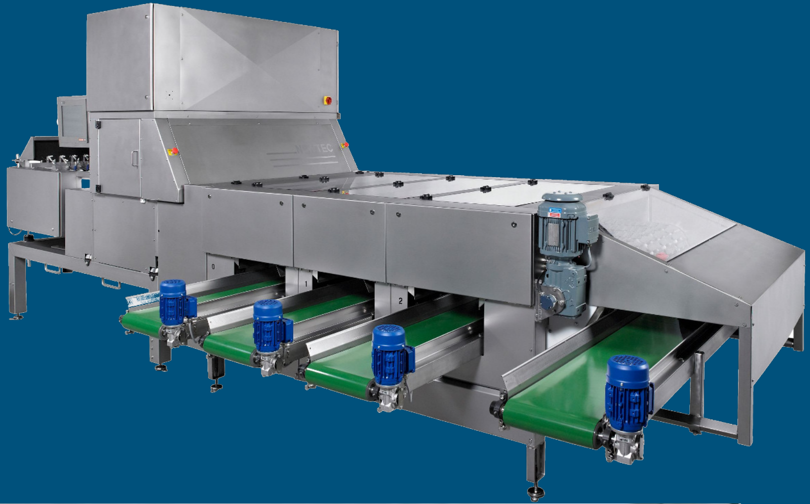
Batch analyzer

Checkweigher

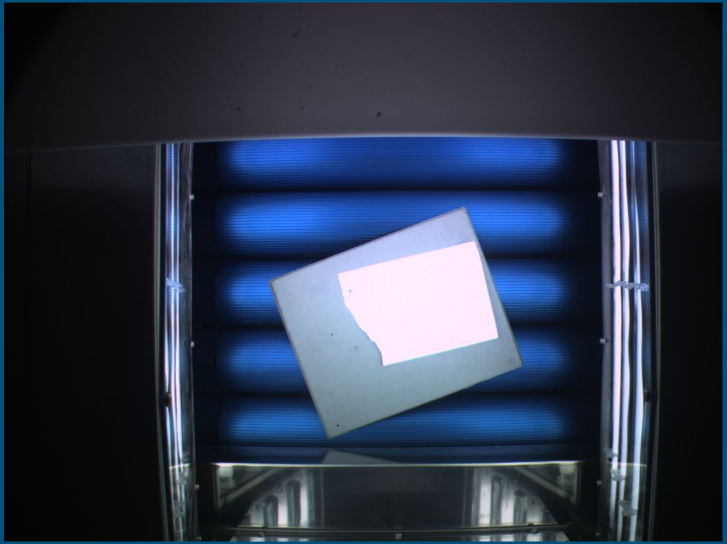
Spectral Camera

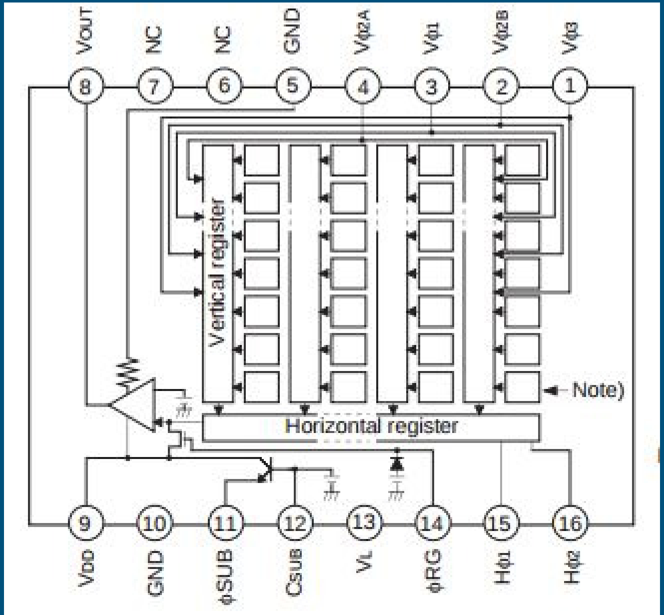
Potato Grader

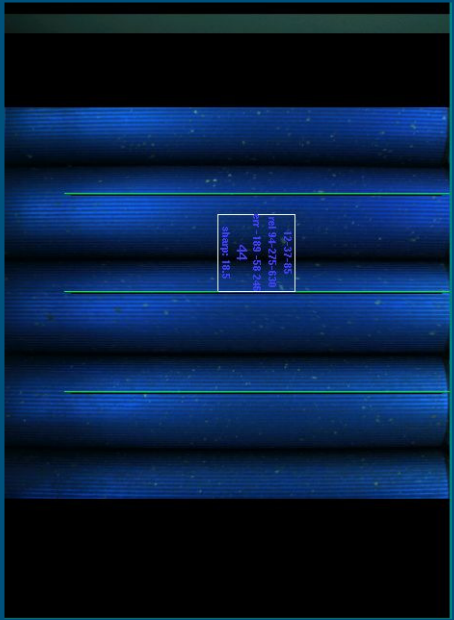




Potato Grader





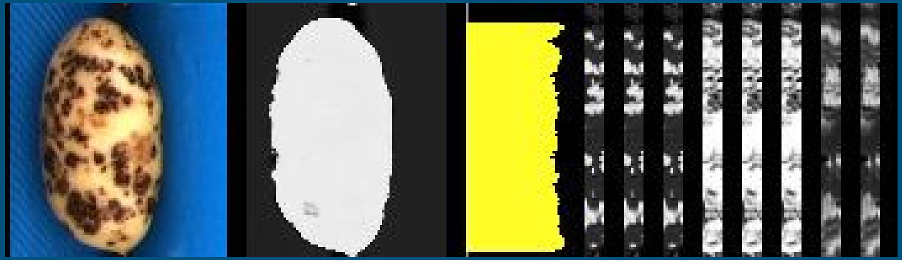


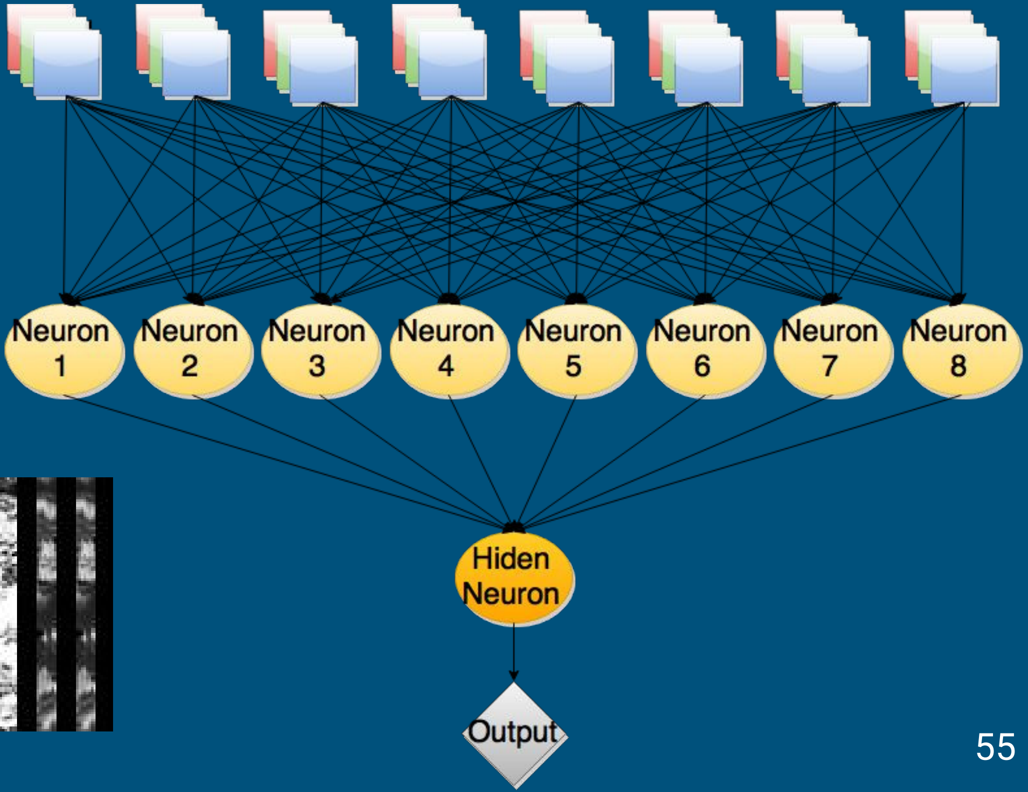
Potato Grader

28 tons per hour

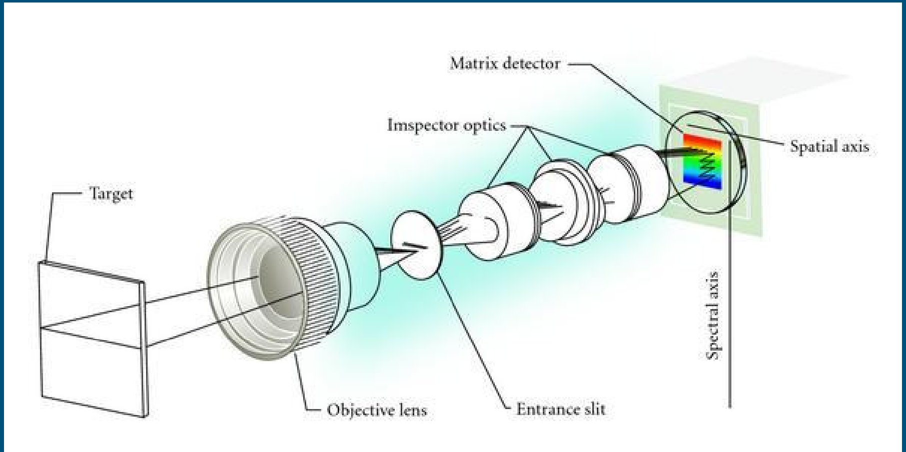
13 categories

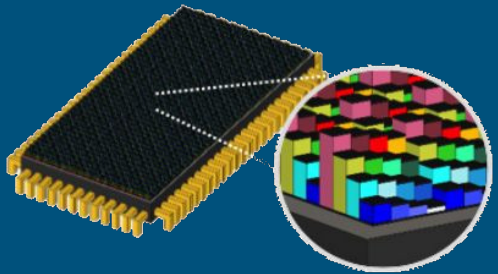
1 mm² resolution

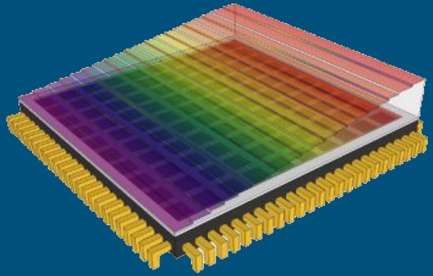




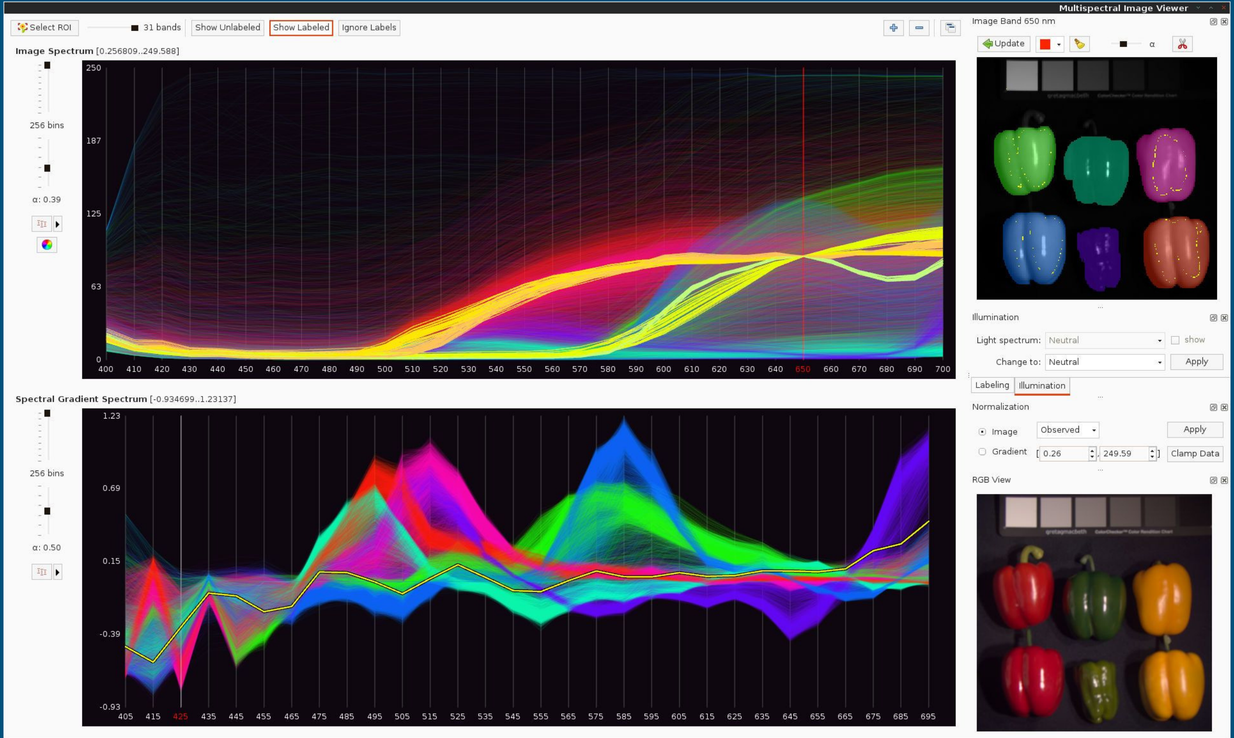
Hyperspectral Camera



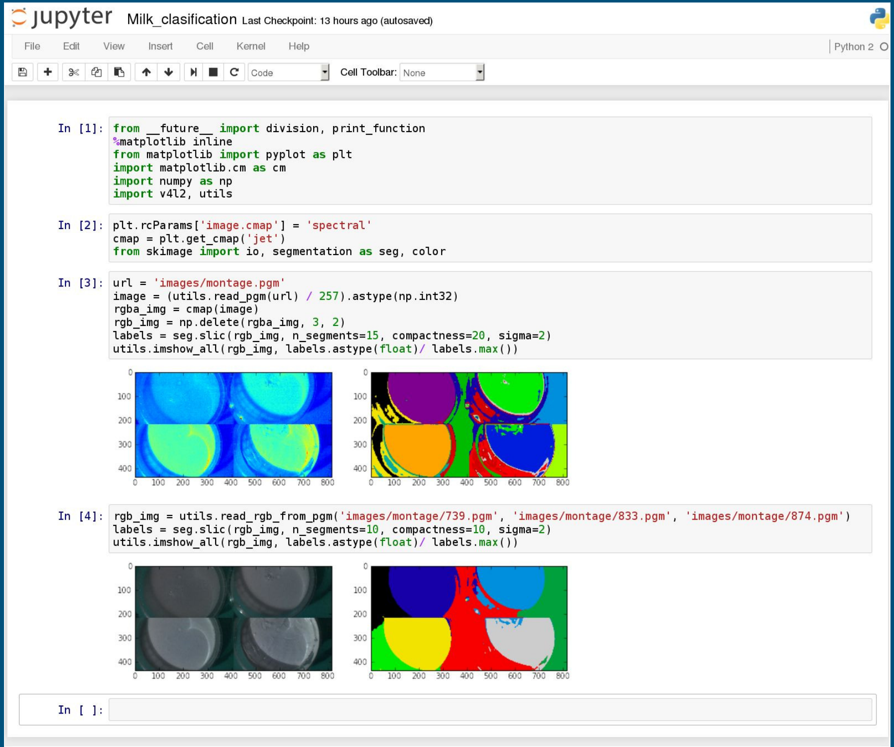




Hyperspectral Camera

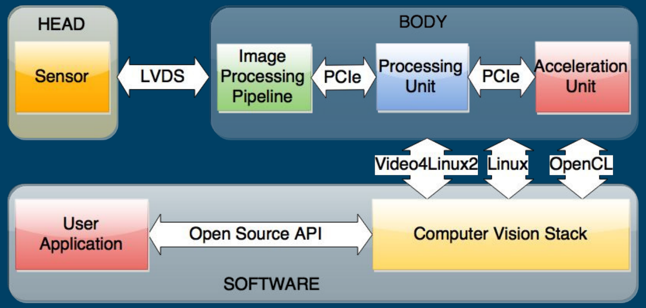


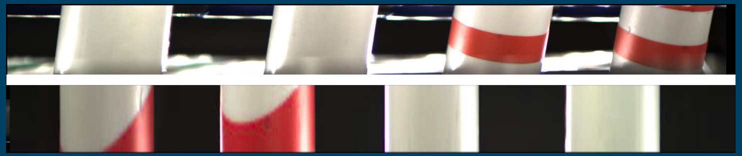
Hyperspectral Camera

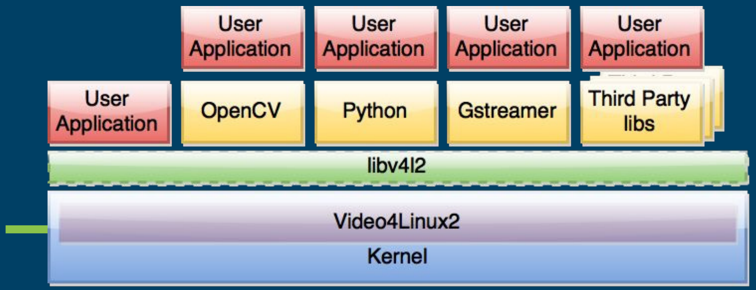


Conclusion and Future Work

★ Original Contributions







Gerald J. Agin Alike System

Pros

Auditable Open Source stack

Integrated DSP

Mature API

Image Preprocessing Capabilities

Real time performance

Highly Parallel Architecture

Easy Programming

~~COTS Hardware~~

Cons

~~Small selection of sensors~~

~~Limited computer resources~~

~~Non updatable hardware~~

~~No direct access to the sensor~~

~~No image preprocessing~~

~~Custom sensor API~~

~~No Image Processing Software Stack~~

~~Slow Development Cycle~~

Scientific Communication

Ribalda, R., De Rivera, G. G., De Castro, Á., & Garrido, J. (2010). A mobile biometric system-on-token system for signing digital transactions. IEEE Security & Privacy, (2), 13-19.

Ribalda, R., De Castro, A., Glez-de-Rivera, G., & Garrido, J. (2008, March). Open and Reconfigurable System on Chip Architecture with Hardware and Software Preprocessing Capabilities Used for Remote Image Acquisition. In Programmable Logic, 2008 4th Southern Conference on (pp. 167-172). IEEE

Kleinert, A., Friedl-Vallon, F., Guggenmoser, T., Höpfner, M., Neubert, T., **Ribalda, R**., ... & Preusse, P. (2014). Level 0 to 1 processing of the imaging Fourier transform spectrometer GLORIA: generation of radiometrically and spectrally calibrated spectra. Atmospheric measurement techniques, 7(12), 4167-4184.

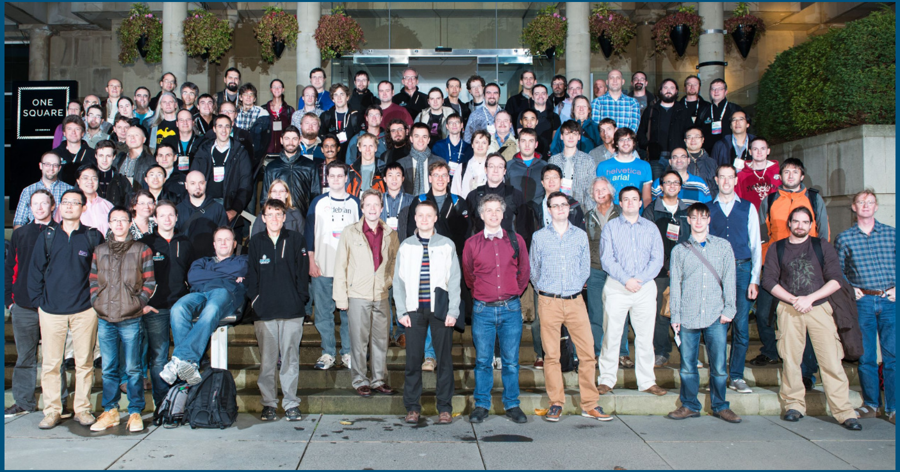
Ribalda, R. The Art of Counting Potatoes with Linux. Embedded Linux Conference Europe (2015). Linux Foundation. Dublin

Specialized Press

Madsen, K. & **Ribalda.R** (2015, February). APU vs. FPGA Was setzt sich bei intelligenten Kameras durch?. inVision. TeDo Verlag Germany.

Madsen, K. & **Ribalda.R** (2015, August) APUs vs FPGAs: The Battle for Smart Camera Processing Supremacy. Electronic Design, Penton Electronics Group, USA

Standardization Process



Ribalda, R. (2013, November) New V4L2 API: Multiple selections. Linux Kernel Media Workshop, Kernel Summit, Linux Foundation. Edinburgh

Ribalda, R. (2014, October) New V4L2 API Proposals: Multiple timestamps & Dead pixels. Linux Media Summit Summit, Linux Foundation. Düsseldorf

Open Source Contributions

Linux Kernel: 172 contributions merged. Including a 9+ year old bug. 2nd Spanish Contributor by number of patches.

U-boot: 25 contributions. Maintainer of Virtex PowerPC boards.

Yocto project: 17 contributions. Supporting organization of the project.

v4l-utils/libv4l2: 7 contributions.

Flashrom: Support for the first board with EEprom memory.

Gerbil: 2 contributions

Clpeak: 2 contributions.

Video Lan Client: 1 contribution.

Future Work

Image Processing Pipeline: High Level Synthesis

Processing Unit: Full Open source

Sensor Interface: USB3

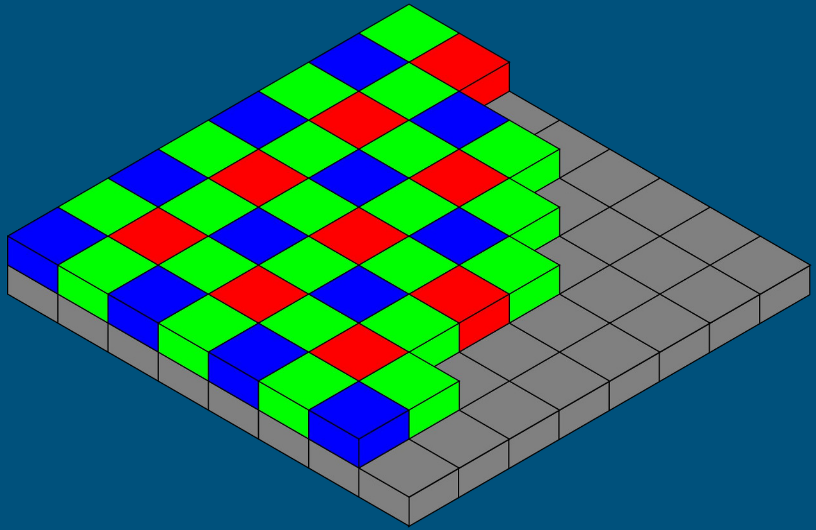
Standardisation

Open Discussion

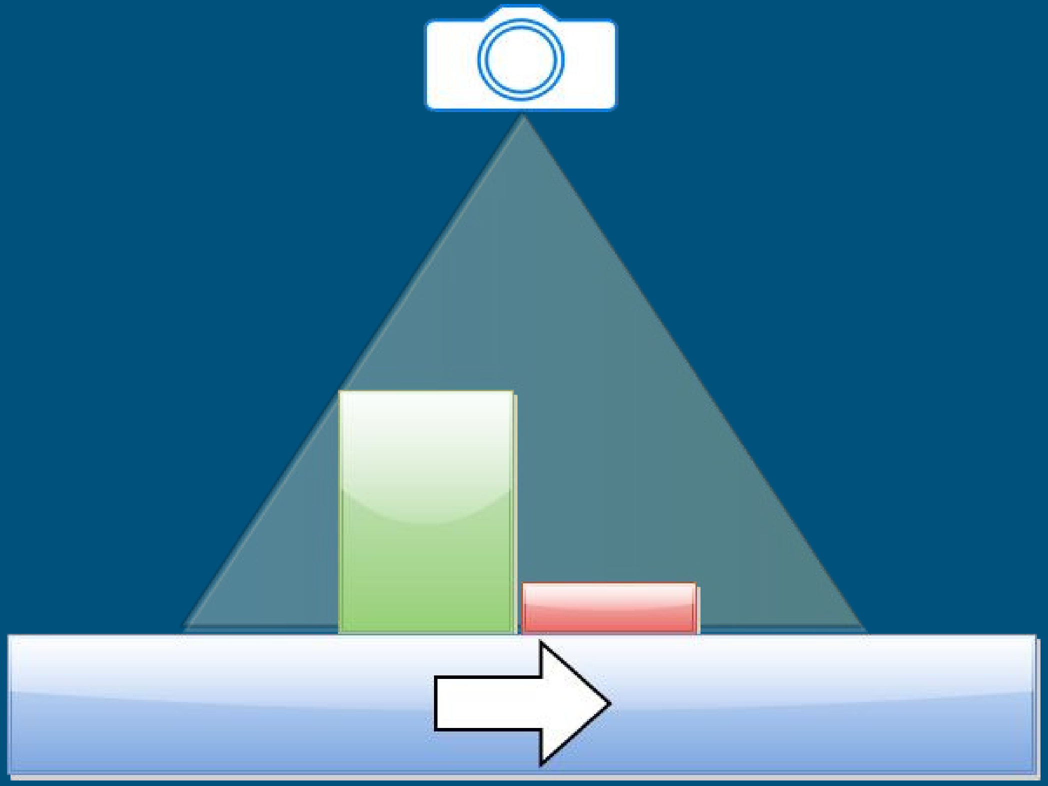
An innovative Vision System for Industrial Applications

Thanks!

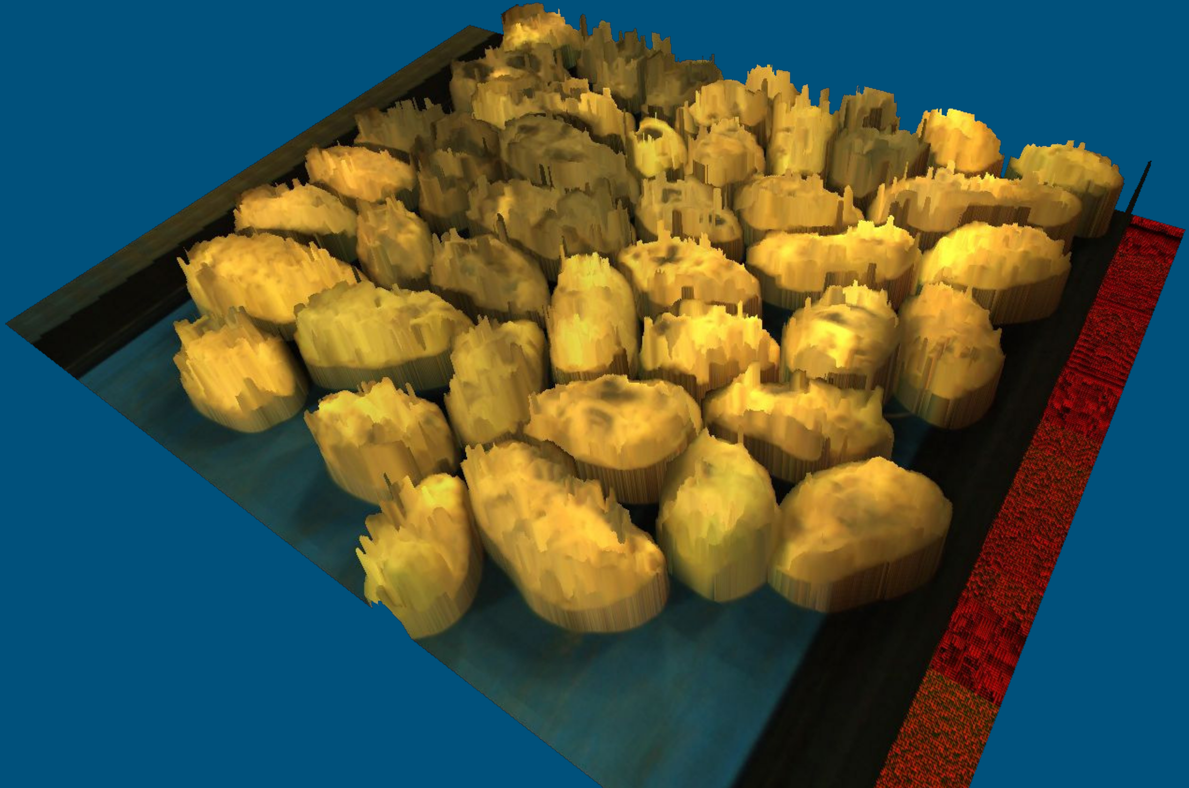
Batch Analyzer



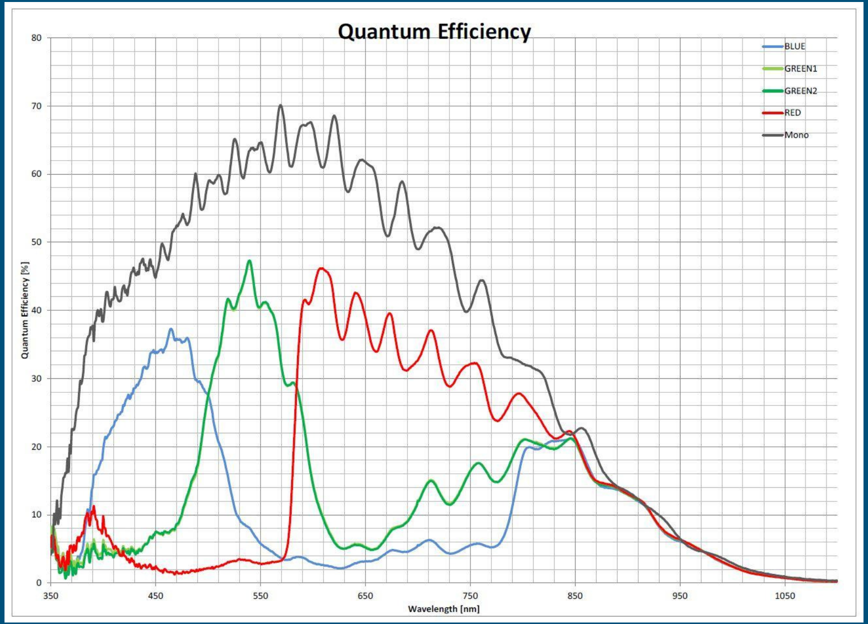
Batch Analyzer



Batch Analyzer



Checkweigher



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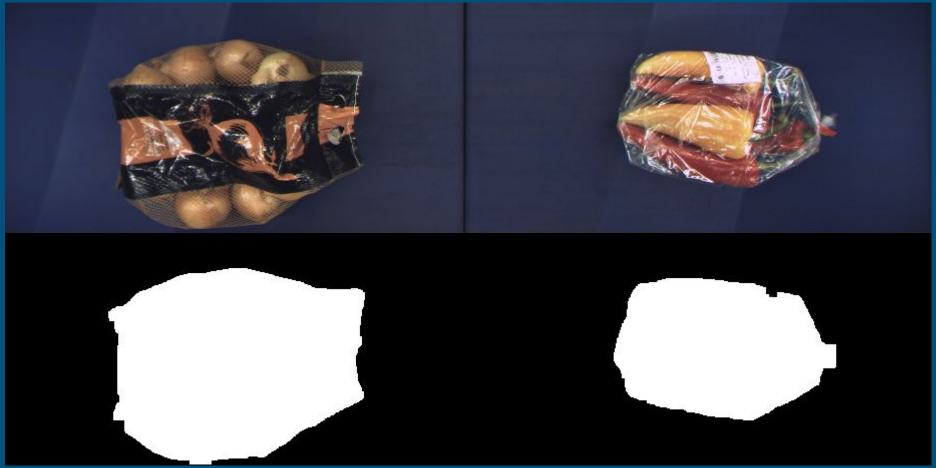
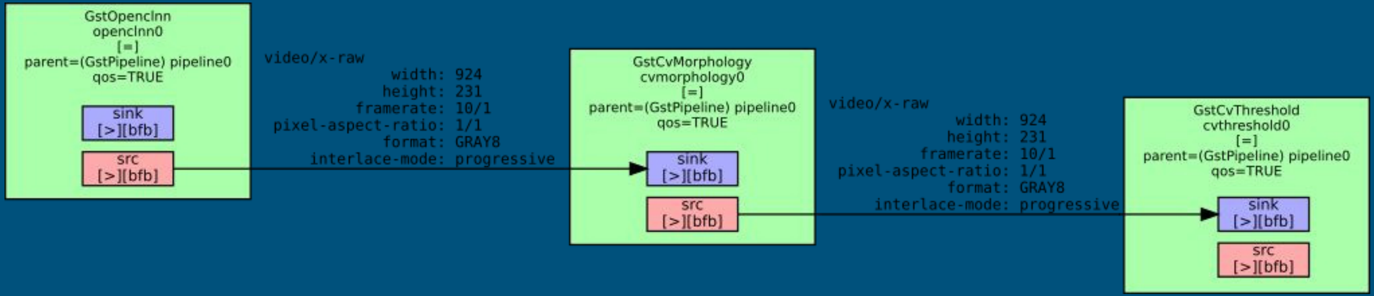
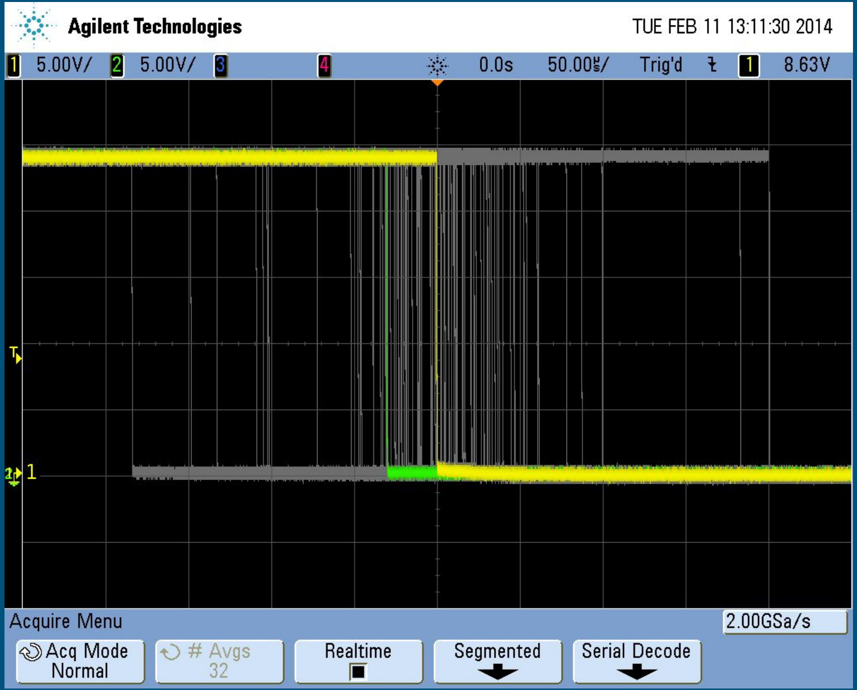


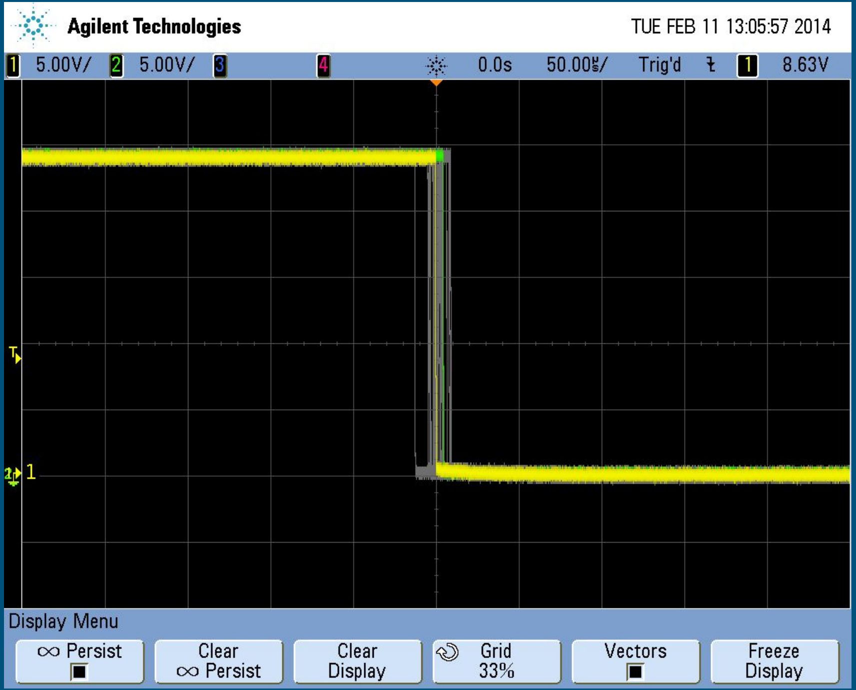


Checkweigher

Clock Synchronization



NTP



PTP